Parallel connection of single-switch three-phase power-factor correction converters for interleaved switching

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Abstract: A circuit for the parallel connection of multiple high-frequency three-phase power-factor-correction converters is proposed which enables their input and output current ripple to be interleaved. Such interleaved operation substantially improves the composite power factor, line-current ripple and output-voltage ripple. The improvement is investigated by developing solutions to circuit state equations which allow the high-frequency content of the line current, as well as the low-order line-frequency harmonics, to be computed. Conclusions drawn from the computed results are verified experimentally using a 1 kW, two-stage, interleaved converter.

1 Introduction

Three-phase power-factor correction preregulators, when implemented with transistor converters comprising six fast switch/diode pairs [1, 2], give a high level of correction performance similar to that achievable with single-phase circuits. The switches of the three-phase converter are, however, only active for 50% of the line-frequency period, and the line currents are, at any instant, conducted by series/parallel combinations of three switches, rather than the one continually active switch commonly found in single-phase circuits. In consequence, the switch-utilisation-ratio (SUR) is about three times lower (see the Appendix, Section 8.1), and a much higher power-semiconductor silicon-area must be used. The device cost associated with introducing power-factor correction into power-electronic systems with a three-phase input is therefore high.

Other factors further increase the relative cost of three-phase power-factor correction preregulators. For example, more complex line-current sensing and control systems are required since three line currents, rather than one, must be actively shaped and controlled to regulate the converter output voltage. Also, the lower switching frequency potential of the high-voltage (i.e. ≥ 1000 V) diodes and switches, increasingly IGBTs, which are required if the converter is to be operated directly from 380 to 480 V supplies, generally limits the reduction in reactive component volume to well below that achievable in single-phase circuits. MOSFETs and resonant-switch circuits may be employed in single-phase circuits to allow operation at switching frequencies at least an order of magnitude higher because voltage levels are generally lower and the switch position in the circuit facilitates their application.

If only unidirectional power flow is required, the disadvantages of the six-switch three-phase converter may be substantially overcome at the expense of some reduction in power-factor correction ability, by using the three-phase single-switch power-factor correction circuit highlighted in Fig. 1. In this circuit, the output voltage is regulated at a higher level than the peak input line-to-line voltage by closed-loop control of the switch duty cycle, and, provided the circuit is operated in the discontinuous inductor-current mode (DICM) at the appropriate constant duty cycle for a given input and output voltage combination, it naturally draws correctly phased discontinuous line-current waveforms with phase-voltage envelopes (see Fig. 2) without the need for line-current sensing and closed-loop current control. Therefore, if the phase voltages are relatively well balanced and their distortion is low, power-factor correction above 0.95 is possible.

From a power-semiconductor utilisation standpoint, the main advantages of the single-switch three-phase circuit are a 2 to 3 factor increase in switch SUR, inherent zero-current turn-on switching which eliminates the high turn-on switching loss associated with high-voltage freewheel-diode recovery, and the potential to easily incorporate the resonant-switch circuits developed for single-phase circuits to reduce turn-off switching loss and noise. The increase in SUR over the six-switch converter arises because the three line currents are controlled by a single switch which is continually active throughout the line-frequency period. The SUR lies below that of the single-phase converter, despite the line-frequency related ripple in the switch current being lower, because the high ripple inherent to DICM operation gives a peak switch current, and hence a switch current rating, that is two to three times the fundamental line-current peak (see Figs. 2 and 3). This cannot be reduced by changing switching frequency, or component values, if DICM operation is to
be maintained. In contrast, the current ripple in continuous inductor-current mode (CICM) converters can be reduced to negligibly low levels by operating at very high $f_{SW}$ values. Even with the high current ripple, however, a worthwhile reduction in SUR is achievable using the three-phase single-switch circuit.

The advantages of the three-phase single-switch circuit and its potential for cost-effective power-factor correction have been acknowledged in the past, and its analysis and operation have been developed a number of times since it was first proposed [3]. Most recently, a rigorous analysis of harmonic suppression performance and complex data for component sizing have been produced [4], and the small improvement in power-factor correction that is possible using a variable $f_{SW}$ control method, rather than a constant $f_{SW}$ method, has been examined [5]. However, one of the main disadvantages of single-switch three-phase circuits, the high level of peak-to-peak line-current ripple produced as a result of the DICM, has not previously been addressed in detail. In previous work, a second-order filter was simply interposed between the AC supply and the converter. The component values required are significantly higher than in CICM converters (i.e. the six-switch type), assuming similar operating conditions, because line-current ripple and salient $f_{SW}$ related frequency components in the line current are more than an order of magnitude higher. An alternative way of addressing the ripple current problem is by operating multiple single-switch converters in parallel (see Fig. 1), and phase-shifting switch conduction so that the composite line-current waveforms comprise the interleaved ripple of the $N$ individual converters. Such interleaved operation has previously been adopted in single-phase DICM.
preregulators [6] and multiple-converter active-filtering systems [7], and shown to have several benefits:

(a) The composite-current-ripple fundamental frequency is multiplied by \( N \).

(b) The input current-ripple amplitude is generally reduced by a factor greater than \( N \), the exact value depending on the duty-cycle.

(c) The switch silicon-area remains approximately constant because the line current is naturally shared equally between individual converters.

(d) A reduction in the lowest \( f_{SW} \)-sideband amplitudes allows some increase in control loop bandwidth because lowpass filters for ripple-amplitude control may be placed at a higher frequency.

The following analysis shows that these benefits may also be exploited in single-switch three-phase converters. However, the direct parallel connection of three-phase converter outputs results in undesirable current circulation, and an additional boost-cell diode must first be added to each converter (see \( D_{b3} \) and \( D_{b4} \), Fig. 1) to isolate boost-cell operation and thus make interleaved operation possible.

2 Single-switch three-phase converter circuit

For analysis, a typical sequence of intermediate states for one single-switch converter is first identified by considering pulse-by-pulse circuit operation (see Figs. 4 and 5). Approximate closed-form solutions are then developed for the state equations of these on the assumption that a high, even-integer, carrier-frequency ratio will be used (i.e. \( f_{SW}/f_{LINE} \approx 50 \)), which will normally be the case for MOSFET and IGBT switches. Thus the full line-current spectrum of switching-frequency harmonics and sidebands, as well as line-frequency harmonics, may be computed, whereas previous analysis methods involving per-phase equivalent circuits [3], part cycle-by-cycle analysis [4], or averaged circuit operation [5], generally, only allowed \( f_{LINE} \) related effects to be considered.

Fig. 4 Typical sequence of equivalent circuits to model operation within switching periods (continued in Fig. 5)

a Switch \( Q \) is on and boost-diode \( D_b \) is off during \( DT_{SW} \) period in Fig. 6a

b \( Q \) is off and \( D_b \) is on during period \( i_{L1} \) in Fig. 6b

Fig. 5 Remainder of sequence of equivalent circuits starting in Fig. 4

a \( Q \) is off and \( D_b \) is on during period \( i_{L2} \) in Fig. 6a

b Both \( Q \) and \( D_b \) are off after \( i_{L3} \) when all inductor currents reach zero

Fig. 6 Characteristic current waveforms during a switching period for constant switching-frequency and variable switching-frequency control methods

a Constant

b Variable

The single-stage converter circuit used in Figs. 4 and 5 comprises: a three-phase power-supply system modelled by sinusoidal sources \( V_a \) to \( V_c \); a fast-recovery-
diode bridge-rectifier; boost-circuit components \( L_d \) to \( L_c \); switch \( Q \); freewheel diode, \( D_h \); sufficient filter capacitance to maintain \( V_o \) virtually constant; and an idealised load represented by \( R_L \). Throughout the analysis, steady-state DICM circuit operation at a fixed duty cycle and high switching frequency is assumed, and the power semiconductor devices and passive reactive components are assumed lossless.

During the conduction of \( Q \), boost inductors \( L_h \) to \( L_c \) are star-connected across the balanced 3-phase supply (see Fig. 4a and period \( DT_{SW} \) in Fig. 6a). Consequently, line currents \( i_L \) to \( i_L \) simultaneously increase at a rate proportional to the instantaneous value of their respective phase voltage. Although the phase voltages vary sinusoidally, they may be assumed constant during a switching period because \( f_{SW} \) is far greater than \( f_{LINE} \). Hence, the inductor-current peaks at the instant of each \( Q \) turn-off are approximately proportional to their respective phase voltages, and follow three-phase sinusoidal envelopes provided the supply voltage is relatively undistorted (see Fig. 2).

Given the balanced nature of the three-phase supply and fixed duty-cycle operation, a constant value of total energy is thus stored in the line inductors during each \( Q \) conduction period. Each time \( Q \) is turned off, the inductor currents commutate to \( D_h \) and decay to zero since the output voltage is always higher than the peak value of the line-to-line input voltage, e.g. \( V_{ab} \). During the complete transfer of stored energy to the RC load-cell (a prerequisite for DICM operation), three distinct regions of inductor-current decay are generally produced (see \( t_1 \) to \( t_4 \) in Fig. 6a). A typical set of equivalent circuits used to model the inductor-reset periods is given in Figs. 4b and 5a.

2.1 Voltage conversion ratio
The voltage conversion ratio \( M \) is defined by eqn. 1, where \( D \) is the switching duty cycle and \( V_{LL} \) is the input line-to-line voltage, and is determined by solving a line-inductor volt-second integral over an \( f_{SW} \) period. This is best performed when one phase voltage is approximately zero, say at \( t = \pi/3 \) (i.e. at \( t = 3.33 \text{ms} \) if \( f_{LINE} = 50 \text{Hz} \); see Fig. 7b), since only two line inductors and phase voltages need be considered. The same conversion ratio must then be obtained at other points in the \( f_{LINE} \) period, during steady-state fixed-duty-cycle operation, because the energy transferred to \( C_d \) from the three line inductors within each \( f_{SW} \) period is constant, and the capacitance of \( C_d \) is usually chosen to give low output ripple and maintain the output voltage approximately constant at \( V_o \):

\[
M = \frac{V_o}{V_{LL}} = \frac{1}{1 - D} \quad (1)
\]

For DICM operation, the minimum permissible duty-cycle value \( D_{min} \) is calculated using the maximum peak line voltage and minimum output voltage likely to be experienced during operation.

2.2 Line-current waveforms
Converter line-current waveforms are generated from approximate solutions to sets of generalised state equations. The coefficients of these depend on where operation lies in a phase-\( a \) \( f_{LINE} \) period. For any current-rise period at sampling instants \( t_i \) in the \( f_{LINE} \) period, Fig. 4a applies, and eqns. 2 and 3, alone, model circuit operation. Zero initial conditions apply for \( i_{Lk} \), as DICM operation prevails.

For \( t_0 \leq t \leq t_1 \),

\[
L \frac{di_{Lk}}{dt} = v_k(t_i) \quad (2)
\]

\[
C_d \frac{dv_o}{dt} = -\frac{V_o}{R_L} \quad (3)
\]

\( k = a, b \) or \( c \), depending on the phase under analysis, and the sampling instants \( t_i \) (see Fig. 7) are given by

\[
t_i = (i + 1 + D)T_{SW} \quad (6), \quad i = 1, 2, \ldots, p, \quad \text{where the switching-pulse number } p = T_{SW}/f_{LINE}.
\]

Peak inductor currents at the end of the switch conduction time \( DT_{SW} \) are approximated by eqn. 4.

\[
i_{Lk}(t_{i1}) = \frac{v_k(t_i)}{L} DT_{SW} \quad (4)
\]

assuming \( L_0 = L_h = L_c = L \). When \( Q \) is turned off at \( t_{i1} \), the inductor currents freewheel through \( D_h \) and the \( RC \) load cell (Fig. 4b) and two periods of inductor current reset generally follow. Initially, all inductors are conducting. The first reset period, \( t_{i1} \) (Fig. 6a) ends when the smallest current reaches zero at \( t_2 \). During \( t_{i2} \) eqns. 5 and 6 apply with initial condition \( i_{Lk}(t_{i1}) \). In eqn. 5, \( \alpha_{ik} \) is a coefficient whose value changes when the phase voltage with the lowest magnitude alters. This is necessary because a different inductor will then reset first and a modified set of equivalent circuits is required. Six sets of \( \alpha_{ik} \) values are required to completely model circuit operation, and these are given in the Appendix (Section 8.3).

For \( t_{i1} \leq t \leq t_{i2} \),

\[
L \frac{di_{Lk}}{dt} = v_k(t_i) - \alpha_{ik} V_o \quad (5)
\]
The second reset period, \( t_{r2} \), involves the two inductors still conducting (Fig. 5a), and persists until all currents have fallen to zero at \( t_{z3} \). Generalised state equations, eqns. 7 and 8, apply for \( t_{r2} \). The coefficients \( a_{2k} \) and \( X'_{k} \) change 12 times throughout the \( T_{sw} \) period as the relative values of phase voltage and hence equivalent circuits change. Values are also given in the Appendix (Section 8.3).

For \( t_{r2} \),

\[
C_{d} \frac{dV_{L}}{dt} = i_{Db} - \frac{V_{o}}{R_{L}}
\]

For the remainder of \( T_{sw} \), the inductor currents are zero, and eqn. 6, alone, describes operation.

Approximate solutions may be generated for the generalised state equations above and allow normalised inductor-current amplitudes and reset times to be calculated for switching instants throughout the \( f_{line} \) period. These are given in the Appendix (Section 8.2) for the first \( f_{line} \) interval, \( 0 \leq \theta_{t} \leq \frac{\pi}{6} \), and must be derived for other intervals to completely describe steady-state circuit operation over an \( f_{line} \) period [8].

A calculated line-current waveform is shown in Fig. 2 for \( f_{line} \) and \( f_{sw} \) values chosen to be 50Hz and 3kHz, respectively, for illustration, and this is expanded at \( \pi/6 \) and \( \pi/3 \) (i.e. 1.67ms and 3.33ms) in Figs. 7a and 7b. In passing through \( \pi/6 \), the relative magnitudes of \( v_{d} \) and \( v_{c} \) change (see Fig. 8a), leading to a change in the relative duration of \( L_{a} \) and \( L_{c} \) reset. Near the second point of interest, \( \pi/3 \), \( v_{c} \) passes through zero. Hence, with \( f_{sw} \) far greater than \( f_{line} \), \( i_{c} \) is approximately zero, and current waveforms are virtually determined by \( L_{a} \), \( L_{b} \), \( v_{d} \), and \( v_{c} \), alone. Since the line-to-line voltage \( v_{ab} \) reaches a maximum at \( \pi/3 \), the peaks and widths of the corresponding current pulses are also maximal. Therefore, operating conditions at this point are put into eqns. 1 and 4, to calculate the maximum inductance that is permissible to place operation at the DICM/CICM boundary.

### 2.3 Line-current frequency spectra

The spectra of the normalised line-current waveforms, computed by the fast Fourier transform algorithm (Fig. 9) [9], show that low levels of \( f_{line} \) harmonics remain. The observable residual low-order harmonics (i.e. 5th, 7th, 11th, etc.) arise because, unlike for the current-rise periods of the current pulses, the current-time areas associated with inductor reset are determined by factors other than the phase voltages, and are not linearly dependent on phase voltage. Hence, they do not accurately follow a sinusoidal distribution, and nontriplen odd \( f_{line} \) harmonics are thus introduced.
The dominant $f_{\text{LINE}}$-harmonic levels vary with duty cycle as shown in Fig. 10. Since these are virtually independent of $f_{SW}$ values above a certain value (i.e. $f_{SW}/f_{\text{LINE}} > 30$) [8], they limit the maximum improvement possible in power-factor correction and also power-converter capacity if the converter is required to comply with harmonic emission standards which set absolute limits. The fundamental $f_{\text{LINE}}$ currents are virtually in phase with the three-phase supply voltages, and hence the power-factor values, shown by the constant switching frequency graph in Fig. 11, arise due to line-current distortion alone.

![Fig. 11: Computed variation in input power factor with duty cycle for single-stage, two-stage interleaved and three-stage interleaved three-phase boost converters for $f_{SW}/f_{\text{LINE}} = 60$](image)

### 3 Variable switching frequency control

The total RMS current associated with residual $f_{\text{LINE}}$ harmonics may be reduced somewhat by using variable-frequency rather than constant-frequency control of the boost-cell switch, as proposed in [5]. This involves controlling the converter switch to minimise the zero-current periods in the discontinuous line-current waveforms (see Fig. 6b). With this control method, the point at which all line currents reach zero is detected and used to start the next conduction period of $Q$. Since the blocking time of $Q$ is dependent on the current reset times $t_{r1}$ and $t_{r2}$, which vary over the $f_{\text{LINE}}$ period, the switching frequency of $Q$, i.e. $1/(DT_{SW} + t_{r1} + t_{r2})$, now varies. The conduction duty cycle of $Q$ also varies cyclically above a minimum value $\delta_{\text{min}}$ [8].

Line-current waveforms for variable-frequency control may also be obtained, as previously described for constant $f_{SW}$ operation [8], to allow a more complete analysis of line-current spectra than in previously used methods [5]. The 5th and 7th residual harmonic levels and the input power factor have been computed from the unfiltered line currents and overlaid in Figs. 10 and 12 for comparison with results for fixed $f_{SW}$ control. Although both the low-frequency $f_{\text{LINE}}$ and high-frequency $f_{SW}$ related spectral content changes, the improvement in power factor, especially at low duty cycle, arises largely because of less reduction in the fundamental line-current amplitude. Reduction in the total RMS current associated with $f_{\text{LINE}}$ harmonics and $f_{SW}$ related components is less marked [8].

4 Interleaved operation of converters

The high level of $f_{SW}$ related ripple in the line currents of the single-switch converter, in particular, produces a significant reduction in power factor. This is generally greater than twice the fundamental line-frequency amplitude (see Figs. 2 and 3) and more than an order of magnitude higher than that commonly found in CICM converters. The higher values of input-filter components required compromise the potential passive-component-volume and dynamic-response advantages of the discontinuous converter. With fixed $f_{SW}$ control, however, this problem may be virtually eliminated by parallel connecting two or more converters and interleaving their switching. Ripple cancellation by interleaving variable $f_{SW}$ waveforms gives less reliable results and hence the variable $f_{SW}$ method of control will not be considered further. The advantages of interleaved converter operation have previously been applied to single-phase power-factor preregulators with DICM [6] and CICM [7] operation, and to six-switch converters [10], but not to three-phase single-switch converters.

A two-stage parallel converter is given in Fig. 1. If the control pulses applied to the main switches are synchronously and optimally phase shifted by half an $f_{SW}$ period, the input and output ripple frequency is effectively doubled and the ripple amplitude is reduced by a factor greater than two (cf. Figs. 2 and 13). As well as alleviating the input and output filtering requirements, the line-inductor and output filter capacitor volume are reduced for a given output power because the total peak energy stored in the circuit inductance is halved. The reduced current-pulse amplitudes and increased ripple frequency in the composite output of the boost cells, also, reduce the excess required in the value and rating of the output filter capacitor, above that determined by $6 f_{\text{LINE}}$ ripple-current considerations alone.

For $N$ interleaved converters the optimal phase difference between boost cells is $1/N$ times the $f_{SW}$ period [6], the peak energy stored in the $3N$ line-inductors is reduced by $1/N$, and input and output current ripple frequency and amplitude are increased to $N f_{SW}$ and reduced below $\Delta I/N$, respectively. In principle, con-
verter passive component volume or single-cell $f_{SW}$ may therefore be progressively reduced by increasing the number of interleaved cells (cf. Figs. 2, 13 and 14).

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\[ \text{trum for interleaved two-stage converter operation, at } f = 3 \text{kHz and } D = 0.5, \text{ showing ripple-frequency multiplication and ripple-amplitude reduction} \]

\[ \text{Computed composite phase-a line-current waveform and spectrum for interleaved four-stage converter operation, at } f_{SW} = 3 \text{kHz and } D = 0.5, \text{ showing ripple-frequency multiplication and ripple-amplitude reduction} \]

\[ \text{Computed composite phase-a line-current waveform and spectrum for interleaved two-stage converter operation, at } f = 3 \text{kHz and } D = 0.5, \text{ showing ripple-frequency multiplication and ripple-amplitude reduction} \]

4.1 Interleaved operation of parallel-connected converters

In principle, any number of single-switch three-phase boost converters may be connected for interleaved switching, provided one additional fast recovery diode per stage is added to prevent undesirable converter interaction, e.g. $D_{q3}$ and $D_{q4}$ in Fig. 1. For without these, when $Q_1$ is on, a proportion of forward current set up in $L_{q1}$ to $L_{c1}$ may return through $L_{q2}$, $L_{q3}$ and $L_{c2}$, and vice versa when $Q_2$ is on.

Normalised line-current waveforms and their frequency spectra are calculated for multiple interleaved switching converters, as previously outlined for the single-stage converter, and are shown in Figs. 13 and 14. Comparing the normalised current waveforms and spectra for the two- and four-stage interleaved converters with the single-stage converter shows not only the multiplication of effective $f_{SW}$, but also the reduction in $f_{SW}$ related current. Principal current-ripple frequency components vary with duty cycle. The total ripple cancellation effect and how it varies with duty cycle is best seen from the input power factor calculated from the unfiltered normalised line current (Fig. 11), since this takes into account all frequency components. Phase displacement of the fundamental line current is negligible; as is the variation in $f_{LINE}$ harmonic distortion with $f_{SW}$, once the carrier frequency ratio is above 30 [8].

Hence, the significant improvement in power factor seen is almost entirely due to the ripple cancellation resulting from interleaved converter operation.

A less marked current ripple and thus power-factor improvement is obtained by adding more than two stages, although the potential to reduce filter and line-inductance volume or decrease the fundamental $f_{SW}$ remains because the ripple frequency to $f_{SW}$ ratio continues to rise. The actual reduction in output-filter-capacitor high-frequency RMS current varies below $1/N$ because of the change in composite ripple shape as well as its amplitude. At duty cycles likely to be used in practical 380–480 V three-phase systems, i.e. $D > 0.5$, the reduction is generally greater than $1/N$ [8].

4.2 Converter component sizing

The previous results apply at any power level because they are based on normalised waveforms. However, to verify them it is necessary to design converters to operate at specific power levels. Different circuit operating conditions may be simulated using the previous analysis technique to produce relatively uncomplicated design data. For example, the maximum permissible line inductance is readily determined from the precalculated graph of peak fundamental line current $I_f$ normalised to a base of peak inductor current $I_{L(max)}$, shown in Fig. 3 and eqns. 1 and 4. The relationship between $I_f$ and $I_{L(max)}$ remains because the ripple frequency to $f_{SW}$ ratio remains virtually constant once the carrier-frequency ratio exceeds a certain value (e.g. $f_{SW}/f_{LINE} > 30$ [8]). A single graph may, therefore, be used to find the maximum allowable line inductance to always give DICM operation. This considerably simplifies the determination of line inductance $L_{c}$ to $L_{c}$, values over previously documented methods [3, 4].

For single power-stage circuit design, the maximum duty cycle is obtained by using eqn. 1 with the minimum operating voltage-conversion ratio likely to be experienced. This fixes an abscissa on Fig. 3 and hence the $I_f/I_{L(max)}$ value. Converter power capacity sets $I_f$, and hence the absolute value of $I_{L(max)}$, and $T_{SW}$ is
fixed by the optimum switching frequency for the power-semiconductor technology used. The maximum value of $L$ is then obtained by solving eqn. 4 at $\omega t_c = \pi/3$, when $v_c$ is zero and a single period of inductor reset occurs (see Fig. 7b).

Normalised circuit current waveforms may also be used to produce average and RMS current for the power semiconductors and other passive components, from which component current ratings and power dissipation may be determined [11].

The design procedure and data are equally valid in the design of single-switch converters for parallel connection, since operation is similar except that total power capacity and peak inductor current are divided by $N$, and line inductance is multiplied by $N$.

![Fig. 15](image)

**Fig. 15** Measured phase-a inductor current and filtered line current and phase voltage for experimental single-stage converter

a Inductor current

b Line current and phase voltage

5 Practical verification of analysis

To validate analytical results and the design methods two single-switch three-phase boost converters were designed for connection and operation as in Fig. 1. Boost-cell components were set at $L_a = L_b = L_c = 170\mu F$, $C_d = 200\mu F$ and $R_L = 60\Omega$ for DICM operation under the following conditions: $V_s = 50V$, $V_o = 245V$, $P_o = 1kW$, $f_{LINE} = 50Hz$ and $f_{SW} = 20kHz$.

The experimental results obtained with these are somewhat marred by distortion and imbalance in the laboratory three-phase supply system used, although this does have the advantage of illustrating the system's vulnerability to supply voltage distortion. Fig. 8a shows signals proportional to the synthesised 87V three-phase supply voltages which were derived from a 415V supply system using an isolation transformer and variac.

Examination of the phase-a discontinuous line-current waveform $i_{La}$ for a single-stage converter on a 50MHz analogue oscilloscope confirmed that operation is fully discontinuous and the system was properly designed. However, the $i_{La}$ waveform included here in Fig. 15a was recorded on a digital oscilloscope, and the crest ripple and apparent incomplete current reset to zero, either side of the sinewave peak, results from the relatively low oscilloscope sampling rate. A second-order input filter effect with $f_B = 5kHz$ is provided by the transformer leakage inductance, and added line-to-line capacitance $C_l$ removes the high-frequency current ripple while producing very little phase shift between line currents and phase voltages, as shown in Fig. 15b. The remaining odd line-frequency harmonics, mainly 5th, are largely unaffected by the 5kHz lowpass filter, and their effect is apparent in the filtered line currents (see Fig. 15b). Spectral analysis of the practical discontinuous line current gave frequency-component amplitudes which were in good agreement with the results predicted by computation [8].

![Fig. 16](image)

**Fig. 16** Measured phase-a inductor current and filtered line current and phase voltage for experimental two-stage interleaved converter

a Inductor current

b Line current and phase voltage

5.1 Practical results for interleaved operation

For interleaved operation, the two single-stage circuits were parallel connected and operated open-loop into a resistive load. The constant duty cycle IGBT drives were phase shifted by $f_{SW}/2$. The composite phase-a
unfiltered and filtered line currents are shown in Fig. 16 and the three filtered line currents are given in Fig. 8b with the corresponding phase voltage waveforms. The line current frequency spectra before and after interleaving are shown in Fig. 17 and confirm that artificial switching frequency multiplication and a high level of ripple reduction is indeed possible in practice. Comparing Figs. 17a and 17b shows that ripple frequency components at the fundamental converter switching frequency (i.e. ~20kHz) are virtually eliminated, and, although converter power capacity has been doubled as shown by the factor of 2 increase in fundamental $f_{\text{LINE}}$ current, the residual line-current ripple at $N_{f_{\text{SW}}}$ (i.e. 40kHz) is low and comparable with levels found in CICM converters. The frequency spectra for the filtered line currents, when expanded, reflect the imbalance in source voltages, impedances and converter per-phase circuits. In consequence, fundamental and harmonic line-current levels differ and low levels of third harmonic are introduced into line currents [8].

**Fig. 17** Frequency spectra computed from unfiltered phase-a line currents in experimental single-stage and two-stage interleaved converters. 

a) Single-stage converter  
b) Two-stage interleaved converter

## 6 Conclusions

By connecting a single-switch boost converter after a three-phase rectifier, and operating it in the DICM mode at constant switching frequency and duty cycle, pulsed line currents with an approximately sinusoidal average current may be naturally drawn from a three-phase supply. Control circuit requirements are relatively simple and, since the circuit employs small reactive components, it is potentially capable of very fast response to changing operating conditions. The disadvantages of the circuit include: the supply voltage distortion has a direct influence on line-current distortion; residual $f_{\text{LINE}}$ harmonics cannot be reduced below a certain level by raising $f_{\text{SW}}$ or control-loop bandwidth, as is the case in principle with six-switch CICM power-factor correction preregulators; the circuit draws pulsed line currents under a sinewave envelope greater than twice the fundamental current amplitude, necessitating heavy input filtering below $f_{\text{SW}}$ and circuit analysis and design to ensure proper DICM operation under a range of operating conditions is difficult.

Some of the disadvantages have been addressed here. A method of analysis is presented and verified which allows both $f_{\text{LINE}}$ and $f_{\text{SW}}$ components of the unfiltered line-current frequency spectra to be computed. As a result, the levels of residual $f_{\text{LINE}}$ harmonics and $f_{\text{SW}}$ related components may both be studied to assess compliance with standards or to design input filters. Also, normalised design graphs have been produced to considerably simplify boost-cell inductor and capacitor selection for DICM operation. The problems associated with switching and drawing high line-current peaks have been addressed by devising a simple method of parallel connecting a number of boost stages and interleaving their switching. With interleaved converters, an equivalent device silicon area is in principle required, and the main reactive-component volume associated with the boost-cell and input-filter reactive components is reduced. Also, good current sharing between converters is naturally obtained.

## 7 References

8 Appendixes

8.1 Switch utilisation ratio

The switch utilisation ratio $SUR$, defined for inverter topologies in [12] and given by eqn. 9, is used here to estimate the relative silicon cost of power-factor correction preregulator topologies:

$$SUR = \frac{(VA)_1}{qVT_I}$$  \hspace{1cm} (9)

$(VA)_1$ is the converter volt-ampere capacity at the fundamental line frequency $f_{LINE}$ and $V_I$ and $I_T$ are the theoretical peak voltage and current ratings, respectively, required by the $q$ converter switches to achieve this, assuming idealised, 100% efficient, converter operation.

$$M = \frac{V_o}{V} = \frac{1}{1 - D}$$  \hspace{1cm} (10)

The power-factor correction preregulators incorporate boost-converter switching cells. Hence, converter output voltage $V_o$ has a direct bearing on switch voltage rating, and the voltage-conversion ratio term $M$ must be incorporated in $V_I$ (see eqn. 10, where $V$ is the peak fundamental line-neutral in single-phase systems and the peak fundamental line-to-line voltage in three-phase systems). Converter switch current rating $I_T$ is determined by the peak controlled current, and, since current ripple increases this, a ripple term $r$ may be incorporated in $I_T$ (see eqn. 11, where $I_S$ is the fundamental input line current and $\Delta I_S$ is the peak ripple magnitude above this):

$$r = 1 + \frac{\Delta I_S}{I_S}$$  \hspace{1cm} (11)

The relative SUR values for (i) the CICM, single-phase, power-factor correction preregulator based on the boost converter; (ii) CICM, three-phase, six-switch converter; and (iii) DICM, three-phase, single-switch converter are given in Table 1. In the CICM converters, current ripple may, in principle, be rendered negligible by choosing a very high $f_{SW}$ value. Hence, a unity $r$ value is used for CICM converters which gives the theoretical upper limit for SUR. In the DICM case, because current ripple is very high and is virtually independent of $f_{SW}$ above a certain $f_{SW}/f_{LINE}$ ratio, it must be taken into account. The variation in current-ripple amplitude with duty cycle must also be considered. Normalised peak-current values for a range of $D$ may be calculated from the data in Fig. 3, and are used to calculate the maximum achievable SUR over the duty-cycle range, $0.1 \leq D \leq 0.8$.

### Table 1: Relative SUR values for correction converters and data used in their evaluation

<table>
<thead>
<tr>
<th>Converter type</th>
<th>Switch number $q$</th>
<th>Power capacity (VA)$_1$</th>
<th>Switch voltage rating $V_I$</th>
<th>Switch current rating $I_T$</th>
<th>Current ripple factor $r$</th>
<th>SUR</th>
<th>SUR/SUR$_{3PH}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CICM Single-phase boost</td>
<td>1</td>
<td>$V_oI_S$</td>
<td>$\sqrt{2}V_oI_M$</td>
<td>$\sqrt{2}I_S$</td>
<td>1</td>
<td>$1/2M$</td>
<td>1</td>
</tr>
<tr>
<td>CICM Six-switch three-phase</td>
<td>6</td>
<td>$3V_oI_S$</td>
<td>$\sqrt{6}V_oI_M$</td>
<td>$\sqrt{2}I_S$</td>
<td>1</td>
<td>$1/6(2/3)M$</td>
<td>0.29</td>
</tr>
<tr>
<td>DICM Single-switch three-phase boost</td>
<td>1</td>
<td>$3V_oI_S$</td>
<td>$\sqrt{6}V_oI_M$</td>
<td>$2I_S$</td>
<td>$0.1/1.5D_{o,0.8}$</td>
<td>$1/1(2/3)I_M$</td>
<td>0.08-0.85</td>
</tr>
</tbody>
</table>


8.2 State equation solutions

Normalisation bases:

$$i_L(t) = i_L(t) I_T, V = (V/L)DT_{SW}, L = L, V = V_p, \phi = a, b, or c.$$  \hspace{1cm} (12)

When the switch is turned off, the first inductor reset period, $t_{1a}$, starts, and the inductor currents decrease over $t_1 < t < t_2$ at rates given by eqns. 5 and the appropriate coefficient values from Table 2. Eqsns. 15–17 give these for the first interval of the $f_{LINE}$ period:

$$\frac{di_{Lan}}{dt} = \sin(\omega t_i) - \frac{M}{\sqrt{3}} \sin(\omega t_i)$$  \hspace{1cm} (13)

$$\frac{di_{Lbn}}{dt} = \sin(\omega t_i) + \frac{M}{\sqrt{3}} \sin(\omega t_i)$$  \hspace{1cm} (14)

These apply until the lowest inductor current reaches zero; for example, see $i_L$ at $t_{12}$ in Fig. 6a. This marks the end of the first inductor reset period, $t_{1a}$. Now, putting eqns. 12 and 15 into eqn. 18 gives $i_L(t)$ values for sampling instants within the first $\pi/6$ interval of the line-current waveforms:

$$i_L(t) + \left(\frac{di_{Lan}}{dt}\right)_{t_{12}}t_{1a} = 0$$  \hspace{1cm} (18)

### Table 2: Coefficients for state eqn. 5 for different intervals of the $f_{LINE}$ period

<table>
<thead>
<tr>
<th>$\alpha_{1a}$</th>
<th>$a$</th>
<th>$b$</th>
<th>$c$</th>
<th>$\alpha_{1b}$</th>
<th>$\alpha_{1c}$</th>
<th>$\alpha_{1d}$</th>
<th>$\alpha_{1e}$</th>
<th>$\alpha_{1f}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/3</td>
<td>1/3</td>
<td>1/3</td>
<td>1/3</td>
<td>-1/3</td>
<td>-1/3</td>
<td>-1/3</td>
<td>-1/3</td>
<td>-1/3</td>
</tr>
<tr>
<td>2/3</td>
<td>2/3</td>
<td>2/3</td>
<td>2/3</td>
<td>1/3</td>
<td>1/3</td>
<td>1/3</td>
<td>1/3</td>
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<td>1/3</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 3: Coefficients for state eqn. 7 for different intervals of the \( f_{\text{LINE}} \) period

<table>
<thead>
<tr>
<th>( \omega t )</th>
<th>0-( \pi/6 )</th>
<th>( \pi/6-\pi/3 )</th>
<th>( \pi/3-\pi/2 )</th>
<th>( \pi/2-2\pi/3 )</th>
<th>( 2\pi/3-5\pi/6 )</th>
<th>( 5\pi/6-\pi )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \alpha_{2a} )</td>
<td>0</td>
<td>1/2</td>
<td>1/2</td>
<td>1/2</td>
<td>1/2</td>
<td>0</td>
</tr>
<tr>
<td>( \alpha_{2b} )</td>
<td>-1/2</td>
<td>-1/2</td>
<td>-1/2</td>
<td>0</td>
<td>-1/2</td>
<td>1/2</td>
</tr>
<tr>
<td>( \alpha_{2c} )</td>
<td>1/2</td>
<td>0</td>
<td>0</td>
<td>-1/2</td>
<td>0</td>
<td>-1/2</td>
</tr>
<tr>
<td>( \chi_a )</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>( \chi_b )</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>0</td>
<td>-1</td>
<td>0</td>
</tr>
<tr>
<td>( \chi_c )</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>-1</td>
<td>0</td>
<td>-1</td>
</tr>
</tbody>
</table>

To determine the duration of the second inductor reset period, inductor currents \( i_{L_{ln}}(t_{22}) \) and \( i_{L_{cn}}(t_{22}) \) are first estimated using eqns. 21-24:

\[
i_{L_{bn}}(t_{22}) = i_{L_{bn}}(t_{11}) + \left( \frac{di_{L_{bn}}}{dt_n} \right)_{t_{12}} t_{ir1n} = 0
\]

\[
\Rightarrow t_{ir1n} = -\frac{\sin \omega t_i}{\sin \omega t_i - \frac{M}{\sqrt{3}}}
\]  

(20)

To estimate \( t_{ir2n} \), phase-b inductor current, \( i_{L_{bn}} \) is considered further. At the end of \( t_{22} \), \( i_{L_{bn}} \) falls to zero and eqn. 27 applies:

\[
\Rightarrow t_{ir2n} = -\frac{\text{sin} \omega t_i}{\text{sin} \omega t_i - \frac{M}{\sqrt{3}}}
\]  

(26)

(26)

To estimate \( t_{ir2n} \), phase-b inductor current, \( i_{L_{bn}} \) is considered further. At the end of \( t_{ir2n} \), phase-b inductor current, \( i_{L_{bn}} \) falls to zero and eqn. 27 applies:

\[
i_{L_{bn}}(t_{22}) + \left( \frac{di_{L_{bn}}}{dt_n} \right)_{t_{22}} t_{ir2n} = 0
\]

(27)

Substituting eqns. 22 and 25 into eqn. 27 gives eqn. 28:

\[
\Rightarrow t_{ir2n} = -\frac{\text{sin} \omega t_i - \frac{M}{\sqrt{3}}}{\text{sin} \omega t_i - \frac{M}{\sqrt{3}}}
\]  

(28)

Using eqn. 28, values for the second inductor reset period, \( t_{ir2n} \), may be estimated at any sampling instant within the first \( f_{\text{LINE}} \) interval. Equations for all salient amplitudes and periods are now available, and solving these allows line-current waveforms and other circuit waveforms to be constructed for the first \( \pi/6 \) interval. To fully compute the line-current waveforms over an entire \( f_{\text{LINE}} \) period as shown in Fig. 2, 12 such sets of equations must be derived and solved [8].

8.3 Generalised state equation coefficients

The values of coefficients \( \alpha_{16}, \alpha_{2k} \) and \( X_k \) in the generalised state eqns. 10–16 are dependent on the interval in the \( f_{\text{LINE}} \) period in which operation is taking place, as shown in Tables 2 and 3.