OPTIMISING SNUBBERS FOR HIGH-CURRENT EMITTER-SWITCHED TRANSISTORS

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INTRODUCTION

A high-current cascode-switch for operation at 100A off a rectified 3-phase 415V supply has been developed, and tested at 80A and 600V to show that a rectified 3-phase 415V supply has been applied to medium-power (10-100kW) phase-legs, operating at ultrasonic chopping frequencies. Fast switching and enhanced ruggedness required at turn-off, considerably reduces the shunt snubbing required. However, reduced current-fall time (50nS to 80A & 600V, di/dt<4500A/µs) demands very hard switching. Transistor voltage clamping to uphold transistor Vceo ratings. At high-current (280A), when circuit parasitic-impedance and di/dt-impedance are significant, it is difficult to exploit the power-loss advantage of soft voltage-clamps (fig.1A), and adaptable voltage-clamps become necessary to avoid impractical hardware-layout and complex compensated clamps. Also, emitter switching does not improve transistor turn-on performance. For good transistor utilization, series snubbing is still required to reduce turn-on power-loss or forward-bias second breakdown, and overcome the limit of transistor turn-off power dissipation.

ANALYSIS OF SOFT VOLTAGE-CLAMP

If transistor turn-off crossover-time is much faster than the reset-time of series-snubber inductance, the circuit of fig.1B describes voltage-clamp operation at transistor turn-off. The most important clamp function is constraining collector-voltage overshoot. The series snubber, capacitor, and emitter connection is assumed, such that loop TR, CC, and Dc inductance is orders of magnitude below other inductances. L3 and L5 represent stray inductance common to loops Cc and Cs and Cs, L5, Dc, CC.

By close connection of Cc and Cs, and by taking a significant storage-time and turn-off crossover-time improvements are obtained with large-area, 1000V transistors. The low crossover-time (~50nS to 80A, 600V) and storage-time (~750nS to 80A, 600V) of emitter-switched large-area transistors makes their application feasible in medium-power (10-100kW) phase-legs, operating at ultrasonic chopping frequencies. Fast switching and enhanced ruggedness required at turn-off, considerably reduces the shunt snubbing required. However, reduced current-fall time (50nS to 80A & 600V, di/dt<4500A/µs) demands very hard switching. Transistor voltage clamping to uphold transistor Vceo ratings. At high-current (280A), when circuit parasitic-impedance and di/dt-impedance are significant, it is difficult to exploit the power-loss advantage of soft voltage-clamps (fig.1A), and adaptable voltage-clamps become necessary to avoid impractical hardware-layout and complex compensated clamps. Also, emitter switching does not improve transistor turn-on performance. For good transistor utilization, series snubbing is still required to reduce turn-on power-loss or forward-bias second breakdown, and overcome the limits of transistor turn-off power dissipation.

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### TABLE 1

<table>
<thead>
<tr>
<th>Trv</th>
<th>L</th>
<th>Vcpn</th>
<th>trin</th>
<th>trvn</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.75</td>
<td>0.41</td>
<td>3.52</td>
<td>5.45</td>
</tr>
<tr>
<td>5</td>
<td>0.70</td>
<td>0.46</td>
<td>2.90</td>
<td>4.34</td>
</tr>
<tr>
<td>10</td>
<td>0.45</td>
<td>0.48</td>
<td>2.49</td>
<td>3.85</td>
</tr>
</tbody>
</table>

### TABLE 2

<table>
<thead>
<tr>
<th>L (nH)</th>
<th>R (Ω)</th>
<th>Vcp (V)</th>
<th>trin (µs)</th>
<th>trvn (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>2.4</td>
<td>150</td>
<td>2.5</td>
<td>3.9</td>
</tr>
<tr>
<td>0.5</td>
<td>2.4</td>
<td>150</td>
<td>2.5</td>
<td>3.9</td>
</tr>
</tbody>
</table>
CLAMP DESIGN WHEN L2 IS SIGNIFICANT

At high chopping-frequency, resistor and wiring peak-voltage results, see fig.7 (L2n=L2/L1): the 5% trim and trin curves are for the L2n=0 circuit. To understand waveform variation with L2n, waveforms produced at L2n-contour intersections with lines of constant Vcpn, line-A; constant \( \xi \), line-B; and constant \( \xi \), line-C (fig.7) are drawn. Figures 8 and 9 show that optimum current and voltage waveforms are obtained near L2n-contour intersection with contour \( \xi=0.8 \). Current and voltage waveforms are given in fig.10 for L2n-contour intersections along the \( \xi=0.8 \) contour. Figure 11 gives waveforms for points on the L2n=0 contour with the same damping factors, \( \xi_0 \), as fig.10. Waveforms in fig.10 approximate more closely to the desired half-sine-wave voltages and quarter-sine-wave currents. Plotting trin and trim for \( \xi=0.8 \) would produce similar curves on fig.7 as the L2n=0 curves shown.

\[ \frac{C_2}{C_1} = \frac{(V_{cpn})^2}{(V_{cpn})^2} \]  

Appendix-2 gives the initial selection procedure for \( R, C, \) and \( L_2 \). Table-2 gives the results of all the appendix-2 examples for comparison. To conclude: the ostensibly troublesome parasitic resistor and connection inductance, which increases the clamp capacitance required, can by itself, or with added inductance, improve inductor reset-time and clamp reset-time. \( \xi_0 \) may be set to lower values than with L2n=0 designs for improved trin, because L2n is effective in reducing the capacitor-voltage exponential-tail. For a more comprehensive soft voltage-clamp design-aid further \( \xi \) contours should be added to fig.7, together with voltage and current fall-time curves for circuit conditions along these.

REFERENCES

APPENDIX 1

Normalised parameters for state equations.

\[ t_n = \frac{\omega_0 t}{\omega_0} \]  
\[ t_l = \frac{l_n}{l_0} \]  
\[ V_{cn} = \frac{V_c}{V_0} \]  
\[ L_2n = \frac{L_2}{L_1} \]

Vcpn = peak capacitor-voltage reached
trim = current, L2n, fall-time or L1 reset-time
trin = total L1 and C reset-time
minimum transistor off-time \( \geq \) trim
minimum transistor on-time \( \geq \) (trim - trin)

Other parameter definitions

\[ \xi = \frac{1}{(2 \xi) V(L1/C)} \]  
\[ \xi_0 = \frac{1}{(2 \xi_0) V(L1/C)} \]

Table 3

<table>
<thead>
<tr>
<th>Vcpn</th>
<th>( \xi )</th>
<th>( \xi_0 )</th>
<th>trin</th>
<th>trv</th>
<th>L2n</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 0.61 )</td>
<td>( 0.98 )</td>
<td>2.4</td>
<td>3.5</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>( 0.69 )</td>
<td>( 0.44 )</td>
<td>1.8</td>
<td>3.6</td>
<td>0.5</td>
<td></td>
</tr>
</tbody>
</table>

The minimum trv value occurs near the intersection of \( \xi=0.8 \) and L2n=0.3 curves in fig.7. Row-1 of Table-3 gives circuit performance. A better compromise between trim and trv exists near the \( \xi=0.8 \) and L2n=0.5 intersection, see Table-3 row-2. Here, trin is reduced by raising trvn, but equal minimum on and off times are obtained. The increased Vcpn necessitates 30% more capacitance according to equ.1.

\[ \frac{C_2}{C_1} = \left( \frac{V_{cpn}}{V_{cpn}} \right)^2 \]  

Analyser using closed form solutions. Analyser using numerical integration.

APPENDIX 2

Example-1 Result of crude design

Set C and R under the following circuit conditions:
1. \( I_o = 200 \mu A \)
2. \( L_1 = 5 \mu H \)
3. \( L_2 = 0 \)
4. \( \xi_0 = 4.0 \mu S \)
5. \( V_{cp} = 150V \)

Using \( 10\% \) trv, \( \xi_0 = 0.75 \)

Performance using graphs with crude design components

For \( V_o < 100 \) \( \xi_0 = 2.2 \mu F \)
For \( V_o < 10 \) \( \xi_0 = 1.4 \mu F \)

Example-2 Design using graphs when L2n = 0

Set R and C for circuit conditions in Example-1. From Table-1 using 10%-fall curves \( \xi_0 = 0.65 \)

Vcpn = \( t_n / (V(L1/C)) \) gives \( \xi_0 = 0.48 \)

trim = 2.49

trv = 3.85

Component values may be further manipulated to obtain the nearest preferred values. Once Vcpn set by new C value, revised value of corresponding \( \xi_0 \) will set trim and trv on fig. 4 & 5.

Example-3 Design using graphs when L2n = 0.5

Set R, C and L2 for circuit conditions in Example-1. Fig.10 shows that a good compromise between trim and trv exists at the intersection of contours: L2n = 0.5 \( \xi_0 = 0.8 \)

Figure 10 gives \( \xi_0 = 1.8 \)

Vcpn = \( t_n / (V(L1/C)) \) gives \( \xi_0 = 0.69 \)

\( \xi_0 = 0.44 \)

\( \xi_0 = 1.0 \mu F \)

\( \xi_0 = 2.3 \mu A \)

Table-3 gives circuit performance. A better compromise between trin and trvn exists at the intersection of contours: L2n = 0.5 \( \xi_0 = 0.8 \)

3.2 10^-6 L1/C 
100A 
50V 
150V 
5pS 
2.2pF
FIG. 1 REDUCTION OF SOFT VOLTAGE-CLAMP TO A SIMPLIFIED EQUIVALENT-CIRCUIT

FIG. 2 CAPACITOR-VOLTAGE WAVEFORM VARIATION WITH DAMPING-FACTOR, \( \zeta \)

FIG. 3 SERIES-SNUBBER CURRENT-WAVEFORM VARIATION WITH DAMPING-FACTOR, \( \zeta \)

FIG. 4 PEAK CAPACITOR-VOLTAGE & DURATION OF VOLTAGE CHANGE, \( t_{v_{\text{max}}} \), VERSUS DAMPING-FACTOR

FIG. 5 PEAK CAPACITOR-VOLTAGE & SERIES-SNUBBER CURRENT FALL-TIME, \( t_{r_{\text{sn}}} \), VERSUS DAMPING-FACTOR

FIG. 6 CAPACITOR-VOLTAGE & SERIES-SNUBBER CURRENT WAVEFORMS ABOUT THE OPTIMUM DAMPING-FACTOR

FIG. 7 PEAK CAPACITOR-VOLTAGE VERSUS DAMPING-FACTOR FOR DIFFERENT RESISTOR INDUCTANCE, \( L_z \), \( \zeta = 0.5 \), \( 0.8 \), \( 1.0 \), \( 1.2 \), \( 1.4 \), \( 1.6 \)