THE AFFECT OF THERMAL PERFORMANCE ON DEVICE CURRENT UTILISATION

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Abstract - A significant improvement in power-semiconductor-device utilisation seems possible if the maximum output current of power-stage could be limited by thermal feedback from the power-converter. To illustrate the potential utilisation benefit obtained in main switching devices, the variation in usable current with operating conditions is examined for several devices applied in a constant-frequency-PWM VVVF inverter, and operated under conditions to keep their junction-temperature constant.

INTRODUCTION

Typical errors that exists in heatsink design calculations are often not precisely known or empirically tested despite the strong influence power-device junction temperature has on failure-rate, and thus power electronics system reliability, and the contribution of the heatsink assembly to overall system size and weight. The likely reasons for this include: the difficulty in accurately predicting or even bracketing device power-loss, given the existence of production-spread and temperature variation in conduction and switching characteristics; the complexity of practical power-loss waveforms; the imprecision in estimated thermal impedance and resistance seen by power devices distributed on a heatsink; and the difficulty in measuring the chip-area-averaged junction-temperature of switched power-devices. As a result of such difficulties, the safety margins built into power-stage and heatsink designs will often be far from optimum.

Some improvement in verifying the operating junction-temperature of devices and achieving tighter designs will inevitably result from better loss prediction and thermal-design verification as simulation tools become more widely tested and developed. However, a greater improvement in optimizing device utilisation, and incidentally system reliability, seems possible from more sophisticated active current-limiting, which limits the maximum output current or power of systems to maintain the junction-temperature (or power dissipation) of the main power-devices below a pre-set level, say 125 °C, on a pulse-by-pulse basis. The effects of changes in device heating and cooling characteristics due to dynamic load changes, variation in operating conditions etc would, thus, be directly measured and safeguarded against, by closed-loop control.

There would be significant practical difficulties to overcome in implementing temperature-regulated active-current-limiting, such as obtaining clean, proportional, die-area-averaged, junction-temperature feedback signals, or on-line monitoring of converter input and output power, without adding significantly to device cost. But prior to tackling these, it is necessary to clearly establish the incentive for developing such a control scheme by considering the potential level of increase in device utilisation. This has been investigated, in principle, by notionally applying a range of medium-power devices in a constant-frequency PWM three-phase inverter application and estimating the maximum usable current that gives a specific junction temperature for a range of varying modulating and switching frequencies.

ESTIMATING DEVICE POWER-LOSS IN INVERTERS

Examining device efficiency and current utilisation level in a PWM inverter, rather than the more common test set-up of a single-ended chopper, involves greater analytical complexity because device current and duty-cycle vary sinusoidally, and the variation in all loss components with current level must be determined and averaged over an output-frequency, f0, period. The averaging, however, becomes relatively simple with high carrier-frequency ratio, p, [i.e. p or f0/(2pfν) ≥ 10], provided conduction power-loss and switching energy-loss equations can be expressed as continuous functions of current, because discrete-equation averages may then be approximated by closed-form continuous-equation averages.

The power-loss in each of the bridge-legs of a 3-phase inverter is the same, assuming steady-state machine operation, and it is only necessary to examine the equivalent circuit for one bridge-leg and load-phase shown in Fig. 1. Also, the inductive load, i.e. the machine-winding, is assumed to draw a pure sinusoidal current since the inverter switching period is usually chosen to be far less than the winding time-constant to give low current-ripple.

The calculation of average bridge-leg power-loss in asynchronous regular-sampled-PWM inverters has been the subject of previous investigations [5-11]. Generally, these either involve the numerical solution of discrete loss equations [5,11], or the use of approximate closed-form solutions to discrete equations [6-10]. The latter method of solution, although inherently less flexible and accurate, avoids the need to generate such complex algorithms for numerical solution by computer, and has been shown [9] to give surprisingly low error for regular-sampled-PWM, provided p is at least 10.

CONDUCTION POWER-LOSS

Switch and diode on-state characteristics are approximated here using conventional piece-wise linear models [ Eqs (1a) and (1b) ] but may be specified as a more precise function of current using simulated or measured device on-state characteristics, if greater accuracy is desired.

\[ i(t) = i(0) + \frac{V}{R} t \]  

\[ v_s(t) = v_{so} + i R \]  

Fig. 1 Equivalent circuit for power-loss estimation; and PWM voltage, its fundamental component, and lagging output current.

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Bridge-leg current at any instant, \( \theta \), of the fundamental output-period is given by Eq (2), where \( \phi = \text{ut} \) and \( \phi \) is the phase difference between the load-current and PWM voltage-waveform fundamental [see Fig. 2].

\[
i(\theta) = I_o \sin(\theta - \phi)
\]  

(2)

Transistor and diode normalised conduction periods at any \( \theta \) are given by Eqs (3a) and (3b), where \( M \) is the modulation index and \( \Delta \theta \) is \( 2\pi \).

\[
\Delta \theta_o = \frac{1}{2} [1 + M \sin \theta] \Delta \theta
\]

(3a)

\[
\Delta \theta_o = \frac{1}{2} [1 - M \sin \theta] \Delta \theta
\]

(3b)

Therefore, net average conduction power-loss over \( 2\pi \) is given by Eqs (4a) and (4b).

\[
P_{con} = \frac{1}{2\pi} \sum_{\theta = 0}^{2\pi} [P_o I_o \sin(\theta - \phi)] \Delta \theta_o
\]

(4a)

\[
P_{con} = \frac{1}{2\pi} \sum_{\theta = 0}^{2\pi} [P_o I_o \sin(\theta - \phi)] \Delta \theta_o
\]

(4b)

Approximate closed-form solutions are obtained by assuming \( \Delta \theta \) tends to zero and using continuous system averages given by Eqs (5a) and (5b).

\[
P_{con} = \frac{1}{2} \int_0^{2\pi} [P_o I_o \sin(\theta - \phi)] \left[ \frac{1 + M \sin \theta}{2} \right] d\theta
\]

(5a)

\[
P_{con} = \frac{1}{2} \int_0^{2\pi} [P_o I_o \sin(\theta - \phi)] \left[ \frac{1 - M \sin \theta}{2} \right] d\theta
\]

(5b)

These, when solved, give the following diode and switch average conduction power-loss equations.

\[
P_{con} = \frac{I_o V_o}{2} \left( \frac{1 + M \cos \phi}{4} \right) + I_o \frac{\phi}{2} \left( \frac{1}{8} M \cos \phi \right)
\]

(6a)

\[
P_{con} = \frac{I_o V_o}{2} \left( \frac{1 - M \cos \phi}{4} \right) + I_o \frac{\phi}{2} \left( \frac{1}{8} M \cos \phi \right)
\]

(6b)

Although these loss equations do not incorporate the effects of third-harmonic addition, which is later assumed to be used, the difference in loss may be shown to be small.

**SWITCHING POWER-LOSS**

Switching loss comprises turn-on and turn-off loss components arising from crossover in device current and voltage waveforms. The heat energy added at each switching interval is now readily measurable with high-bandwidth digital oscilloscopes, which perform waveform multiplication and integration to give instantaneous power and energy change [see Fig. 2], and increasingly graphs of switching energy versus current are being supplied by device manufacturers. However, where possible, such direct loss measurements are used. For devices for which loss data is unavailable, switching energy is estimated from switching time data.

**Turn-off switching energy**

Power-device switching performance is often estimated from turn-off current fall, \( t_{r/o} \). However, experimental and published switching waveforms generally show that 50% or more of the turn-off loss occurs during the voltage rise with high-voltage devices. Therefore, if switching crossover time measurements, \( \tau_{c/o} \), are unavailable, Eq (7b), rather than Eq (7a), is used for loss estimation. The 0.8 factor arises due to measurement at 10 or 90% levels.

\[
W_{con,off}(\theta) = \frac{1}{2} I_o I'_o \left( t_{c/o} \right) \frac{V_o}{0.8}
\]

(7a)

\[
W_{con,off}(\theta) = V_o I'_o \left( t_{c/o} \right)
\]

(7b)

Where switching energy-loss measurements do exist, the relationship between \( W_{con,off} \) and switched current at any instant may be approximated by Eq (8) in many cases, where \( W_o \) is the turn-off energy-loss at a reference current value \( I_o \) and \( n \) is the gradient of the loss graph when plotted on logarithmic axes.

\[
W_{con,off}(\theta) = \frac{I_o}{I_{con}} W_o
\]

(8)

Loss graphs for many of the devices considered later are plotted from published data in Fig. 3. Appendix 1, Table 2 gives further device details.

**Fig. 3 (a) Approximate turn-off energy-loss versus switched-current graphs for various devices after parabolic curve fit**

With sinusoidally modulated current \( W_{con,off} \) at any switching instant is given by Eq (9), and Eq (10) gives the total average power-loss. The remaining integration in Eq (10) cannot be solved explicitly and must be approximated by numerical solution.

\[
W_{con,off}(\theta) = \frac{I_o V_o}{2} \left( I_o - \sin \theta \right) W_o
\]

(9)

\[
P_{con,off}(\theta) = \frac{I_o V_o}{2\pi} \left( \frac{I_o}{I_{con}} \right) W_o \frac{1}{2} \int_0^{2\pi} \sin \theta d\theta
\]

(10)
The evaluation of average power-loss relies on specifying switching energy-loss as a continuous function of current which is then easily integrated. It should be noted that the derived loss equations, such as Eqs (8) to (10), are merely examples, and their form, as well as their coefficients, may be adjusted for greater accuracy or new devices.

Turn-on switching energy

The variation in turn-on energy-loss with current, $W_{Qsw_{on}}$, may also be approximated by Eq. (8). Where directly measured $W_{Qsw_{on}}$ data is unavailable, $W_{Qsw_{on}}$ may be estimated using diode reverse-recovery charge, $Q_{in}$ data.

With a stiff drive circuit and little series parasitic-inductance, switch turn-on waveforms, with current freewheeling in a fast-recovery diode, are similar to those in Fig. 2, where $Q_{in}$ is assumed to be fully discharged while the switch voltage, $V_{gs}$, is high at approximately, $V_{gs}$.

$W_{Qsw_{on}}(t) = \frac{1}{2} \int_{I_{on}}^{I_{on}} \frac{Q_{in}}{dI} \sin \theta d\theta$  \hspace{1cm} (11)

With modulated current $W_{Qsw_{on}}(t)$ must be averaged over an output frequency period. Recovery $dI/dt$ is assumed sufficiently high (>400 A/µs), such that $Q_{in}$ approaches the total stored charge in the diode, and is approximately proportional to forward current. $Q_{in}$ is then given at any current by Eq. (12a), where $Q_{in}$ is the recovered charge at a reference current $I_{ref}$, and, for sine-weighted PWM, Eq. (12b) gives $Q_{in}$ at each switching instant, $b$.

$Q_{in}(\theta) = \frac{I_{on}}{I_{on}} Q_{in}$ \hspace{1cm} (12a)

$Q_{in}(t) = \frac{I_{on}}{I_{on}} Q_{in} \sin \theta$ \hspace{1cm} (12b)

Fig. 3 Measured turn-on energy-loss (cont.) for BSM50GB100D with loss estimated from $Q_{in}$ (dash) with correction for stray-inductance associated volt-drop

A turn-on power-loss graph derived using Eq. (11) with a single $Q_{in}$ measurement, is overlaid on a curve fit to manufacturer's $W_{Qsw_{on}}(t)$ data in Fig. 3. Compensating for stray inductance in the energy-loss calculation is necessary and allows the error to be reduced to ~30%.

With sinusoidal load-current, $P_{Qsw_{on}}$, at any switching instant is given by Eq. (13), which gives Eq. (14) when averaged over $2\pi$.

$P_{Qsw_{on}}(\theta) = \frac{I_{on} V_{on}}{2} \int_{I_{on}}^{I_{on}} \frac{Q_{in}}{dI} \sin \theta + \frac{I_{on}}{2} \frac{Q_{in}}{2dI} \sin \theta$ \hspace{1cm} (13)

$P_{Qsw_{on}} = \frac{I_{on} V_{on}}{2} \left[ \frac{I_{on}}{2} \frac{Q_{in}}{dI} \sin \theta + \frac{I_{on}}{2} \frac{Q_{in}}{2dI} \sin \theta \right]$ \hspace{1cm} (14)

When a graph of $W_{Qsw_{on}}$ measurements is available, and a parabolic-curve approximation to it using Eq. (15) is possible, $P_{Qsw_{on}}$ is obtained by averaging Eq. (15) over $2\pi$ to give Eq. (16), as previously performed for $P_{Qsw_{on}}$.

$W_{Qsw_{on}}(t) = \frac{I_{on}}{I_{on}} W_{on} \sin^2 \theta d\theta$ \hspace{1cm} (15)

$P_{Qsw_{on}} = \frac{I_{on} V_{on}}{2} \left[ \frac{I_{on}}{2} \frac{W_{on}}{\sin^2 \theta} + \frac{I_{on}}{2} \frac{W_{on}}{2 \sin^2 \theta} \right]$ \hspace{1cm} (16)

Total power-loss

The total conduction and switching loss produced by a bridge-leg switch-diode pair, $P_{anh}$, may now be calculated by collecting power-loss terms as shown in Eq. (17). Note, that diode switching loss is assumed negligible, at this point. Where parabolic switching-loss equations are appropriate, $P_{anh}$ and $P_{anh}$ are given by Eqs (18a) and (18b).

$P_{anh} = P_{anh} + P_{anh} = P_{anh} + P_{anh}$ \hspace{1cm} (17)

$P_{anh} = \frac{I_{on} V_{on}}{I_{on}} \left( \frac{1}{\pi \cos \theta} + \frac{M}{3 \pi} \cos \theta \right) + \frac{I_{on} V_{on}}{2} \left[ \frac{W_{on}}{\sin^2 \theta} + \frac{W_{on}}{2 \sin^2 \theta} \right] \hspace{1cm} (18a)$

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Net inverter power-stage efficiency, $\eta_{INV}$, is then given by Eq. (19), where $S_o$ is inverter apparent output power.

$\eta_{INV} = \frac{S_o \cos \phi}{S_o \cos \phi + 6 P_{anh}}$ \hspace{1cm} (19)

DERATING POWER DEVICES

Power devices must be operated below their absolute maximum ratings in most applications for an acceptable service life [21, 22]. Current, voltage and power, or junction-temperature, derating must also be performed to allow for production spread in device characteristics, tolerance in design calculations, line-voltage surges, and cost effective heatsink design.

Current derating

The most significant current derating arises from the impracticality of maintaining device case temperature, $T_c$, at 25°C, i.e. the case temperature for which rated device-current is often specified, hereafter termed $T_{c(max)}$. Power devices are normally operated with $T_{c(max)}$ at 70-80°C at maximum ambient temperature to keep heatsink requirements practical while allowing reasonable device utilisation. For case temperatures above 25°C, power-loss must be linearly derated from the maximum allowable value at $T_{c(max)}$, $P_{anh}$ according to Eq. (24), to keep junction temperature, $T_J$, at or below $T_{J(max)}$, which is usually 150°C.
A stress-ratio derating is then indirectly applied by reducing operating \(T_J\) below 150°C to give reasonable equipment service life. A value of \(T_J=110^\circ C\) will be used here as the maximum working junction temperature, \(T_{J(max)}\), based on recommendations for non hermetically sealed packages [21].

**TRANSIENT THERMAL IMPEDANCE CONSIDERATIONS**

From the maximum permissible average device power-loss at \(P_{Q(avg)}\), \(P_Q\) \((T_{J(max)})\), the maximum permissible switch current is readily obtained for rectangular current pulses of width \(t_o\) and duty-cycle ratio \(D\) from Eq (25) by solving for \(I_o\),

\[
P_Q(I_o) = \left(\frac{T_{J(max)} - T_{J(\infty)}}{Z(t_o, D)}\right) P_Q(T_{J(max)})
\]

Modifying Eq (25) to include diode loss and device-case-to-heatsink thermal resistance, \(R_{th,dc}\), across which 5-10°C may be dropped, thus rendering it usable with bridge-leg modules, gives Eq (26). This is, henceforth, used to determine maximum \(I_o\) by assuming heatsink surface, \(T_{h}\), rather than case, \(T_J\); temperature is limited to 70°C.

\[
P_Q(I_o) = \frac{T_{J(max)} - T_{J(\infty)}}{Z(t_o, D)} R_{th,dc} + T_{J(\infty)}
\]

In sine-weighted PWM inverters, device quasi-instantaneous power pulses, obtained by averaging instantaneous power-loss over each \(f_{sw}\) switching period, approximate to sine pulses as shown in Figs. 4 and 5, and an equivalent rectangular power-pulse with the same amplitude and area may be used to give a conservative estimate of heating effect [23, 24]. Solving for \(I_o\) that gives \(T_J=110^\circ C\) or any other \(T_J\) for given \(f_{sw}\) and \(f_o\) values, therefore, proceeds by putting total average transistor and diode loss, \(P_Q\) and \(P_D\), expressed in terms of \(I_o\), in Eq (26), and then solving for \(I_o\) assuming \(P_Q\) originates in a rectangular pulse of amplitude \(nPQ\) and width and duty-cycle \(t_o = 1/nf_o\) and \(D = 1/\pi\), since a rectangular pulse of such dimensions produces the same heating effect as a sine pulse of width \(1/2f_o\) duty-cycle \(1/\pi\), and amplitude \(\pi P_Q\).

**EVALUATION OF USABLE DEVICE CURRENT**

The evaluation of usable current is most simply determined by calculating device loss and \(T_J\) for each \(f_{sw}\) or \(f_o\) value over a range of operating conditions as inverter \(I_o\) is increased, as shown in Fig. 6 and collecting all the \(I_{(\infty)}\) values giving the required \(T_{J(\infty)}\). This is exemplified for the Darlington BJT module in Fig. 7 where \(I_{(\infty)}\) variation with \(f_o\) and \(f_{sw}\) are given. The corresponding net inverter efficiency values may be similarly collected and plotted.

**Fig. 5** (a) High-speed IGBT, MG150Q2YDI, (b) IGBT, BSM150GB100G and (c) MOSFET, BSM191C quasi-instantaneous conduction and switching power-loss components for \(f_{sw}=20kHz\), \(f_o=50Hz\) and \(T_J=110^\circ C\) operation at peak output current.

**Fig. 6** Darlington MG150M2YKI (a) bridge-leg transistor and diode power-loss components and (b) junction temperature and inverter efficiency versus peak inverter output current.

This is exemplified for the Darlington BJT module in Fig. 7 where \(I_{(\infty)}\) variation with \(f_o\) and \(f_{sw}\) are given. The corresponding net inverter efficiency values may be similarly collected and plotted.

**Fig. 7** Darlington BJT, MG150M2YKI maximum peak usable inverter output current \(I_{(\infty)}\) versus (a) inverter output frequency \(f_o\) with \(f_{sw}=5kHz\) and (b) inverter switching frequency \(f_{sw}\) with \(f_o=50Hz\) for \(T_J=110^\circ C\).
The increase in $I_{(\text{on, max})}$ with $f_d$, seen in Fig. 7a, results from the improved filtering effect of package thermal inertia and reduced $T_j$ ripple. Usable $I_{(\text{on, max})}$ is at least 50% higher at $f_d = 50$Hz than at $f_d = 0.5$Hz, making adaptable current limiting of considerable benefit in VVVF applications to enable full device utilisation.

The rapid decrease in $I_{(\text{on, max})}^*$ with $f sw$, seen in Fig. 7b, results from increasing switching-loss. A simple relationship between $I_{(\text{on, max})}^*$ and $f sw$ is not specifiable, even though switching loss varies proportionally with frequency, because conduction and switching loss vary faster than proportionately with current. Hence $I_{(\text{on, max})}^*$ decreases more slowly than in inverse proportion to $f sw$.

From Fig. 7 it is seen that for operation at $f sw = 5$kHz and $f_d = 50$Hz, $I_{(\text{on, max})}^*$ is limited to 71A for the Darlington BJT. This is confirmed by practical experience because the device is recommended for and applied in 33kVA, 415V AC inverters [13, 15] with a maximum continuous r.m.s. output-current capability of 49.5A i.e. with 110% continuous current overload because the nominal rated output is 45A r.m.s., which corresponds to an $I_{(\text{on, max})}^*$ of 70A.

Making allowance for production spread in device characteristics necessitates further current derating if typical data sheet on-state voltage and switching loss coefficient values are initially used. Maximum on-state voltage and switching parameters are often specified and were used, whenever available, in determining the presented device usable current values.

Generally, typical $125^\circ$C conduction and switching loss data is used without scaling for device utilisation prediction and comparison at $110^\circ$C. Similarly, $125^\circ$C freewheel-diode conduction and reverse-recovery data is used to simplify the determination of $I_{(\text{on, max})}$ in bridge-leg modules. Precise determination of freewheel-diode $T_j$ is usually prevented by the absence of any data to calculate the switching-loss associated with diode current-fall and voltage-rise. Estimation of $T_j$ [see Fig. 6b] will therefore be low.

Usable switch current is not only dependent on switching and conduction loss, but, also, on allowable $I_d$ stress-factor, device package and heatsink thermal performance, production tolerance in characteristics, and freewheel-diode reverse-recovery performance. The switch-current derating calculation, therefore, cannot be reduced to a simple multiplication by a stress-factor, but is obtained from a more complex calculation, the aim of which is to find the $I_{(\text{on, max})}$ corresponding to the power-loss giving the derated maximum junction temperature. By operating at or below $I_{(\text{on, max})}^*$, it is unlikely that any of the absolute maximum peak, average or r.m.s. device currents will exceed the manufacturer recommended derated values, but this should be confirmed.

**VARIATION IN DEVICE UTILISATION**

Maximum usable peak inverter current, $I_{(\text{on, max})}^*$, is evaluated for a range of 1000-1200V, 150A device technologies, when operated with $T_j$ at $110^\circ$C in a 415V AC off-line inverter. Power loss graphs are given in Fig. 8 for the devices when operated in an inverter at the same, $f_d$, and illustrates differences in the levels of conduction and switching power-loss and their temperature sensitivity.

![Power Loss Graphs](image)

**Usable current of switches at high frequency**

The variation in usable $I_{(\text{on, max})}^*$ and inverter power-stage efficiency, $\eta_{\text{INV}}$ with $f_d$ and $f sw$ is shown in Figs 9 and 10, and spot values for operation at $f_d = 50$Hz, $f sw = 20$kHz and $T_j = 110^\circ$C are given in Table 1. The low $R_{\text{on}}$ of the cascode-switch, 150A, single-BJT, compression-capsule package allows its use at about twice the $I_{(\text{on, max})}$ of all other devices except the MOSFET switch, irrespective
of \( f_s \) and \( f_{sw} \) as seen in Figs 9a and 10b. The high MOSFET \( f_{sw}^{(\text{on)}} \) arises despite high power-loss because a 1000V, 150A switch rating is only achievable using five parallel connected 1000V, 28A modules which gives very low \( R_{\text{ac}} \) and \( R_{\text{achi}} \) values [Appendix-1].

<table>
<thead>
<tr>
<th>DEVICES</th>
<th>( I_0 ) (A)</th>
<th>( I_{300} ) (A)</th>
<th>( I_{500} ) (A)</th>
<th>10V (W)</th>
<th>( R_{\text{AC}} ) (%)</th>
<th>( R_{\text{achi}} ) (%)</th>
<th>( I_{\text{D}} ) (A)</th>
<th>( Z_{\text{in}} ) (%)</th>
<th>( R_{\text{AC}} ) (KW)</th>
<th>( R_{\text{achi}} ) (KW)</th>
</tr>
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<tbody>
<tr>
<td>GTR+MOSFET CASCODE</td>
<td>83</td>
<td>147</td>
<td>239</td>
<td>365</td>
<td>96</td>
<td>159</td>
<td>427</td>
<td>953</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>BSM151C MOSFET</td>
<td>86</td>
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<td>148</td>
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Table-1 Maximum usable current, \( I_0 \), for \( T_J = 110^\circ \text{C} \); total average switch power-loss, \( P_{\text{avg}} \); net inverter efficiency, \( \eta_{\text{net}} \); device thermal resistances and effective normalised impedances.

The higher \( I_{\text{sw}}^{(\text{max)}} \) of the IGBT, BSM150GB100D, [Fig 10a] over the high-speed IGBT, MG150Q2Y511, similarly, arises despite lower efficiency, illustrated in Fig 8, due to lower \( R_{\text{AC}} \). The increase in \( I_{\text{sw}}^{(\text{max)}} \) with \( f_s \), seen in Fig 9, arises because of improved thermal filtering and shows that adaptive active-current-limiting would optimise device utilisation in VVVF applications, irrespective of device type.

Fig 9a gives usable \( f_{sw}^{(\text{on)}} \) assuming all switching loss is eliminated, and shows that for most devices a factor of three improvement appears possible at 20kHz. This is of interest because it gives an indication of the potential gain in device utilisation obtainable, in principle, using snubber networks or soft switching.

The ordering of devices in Fig 9a is determined by on-state voltage and package thermal performance. The higher \( f_{sw}^{(\text{on)}} \) is obtained with the single stage BJT in the cascode configuration, the low-saturation-voltage IGBT has the higher \( f_{sw}^{(\text{on)}} \) of all IGBTs, and the MOSFET with its high \( R_{\text{sw}}^{(\text{on)}} \) has a relatively low \( f_{sw}^{(\text{on)}} \) compared with the faster IGBTs, despite good package thermal performance, because of its significantly higher on-state voltage.

If \( f_s \) is held constant at 50Hz and \( f_{sw} \) varied, maximum usable current \( I_{\text{sw}}^{(\text{max)}} \) varies for the devices as shown in Fig 10a. Corresponding \( \eta_{\text{net}} \) graphs are given in Fig 10b. Fig 10a illustrates the penalty associated with high \( f_{sw} \) inverter operation because, except for MOSFETs, the fall off in usable \( f_{sw}^{(\text{on)}} \) is very rapid with increasing \( f_{sw} \), even for the high-speed IGBT.

The main point of this section has been to show the variation of usable device current that is possible over a range of operating conditions in an application. Choice of device, and the optimum \( f_{sw} \) range over which it may be used, is facilitated by comparing \( I_{\text{sw}}^{(\text{max)}} \) and \( \eta_{\text{net}} \) in the actual application, especially with varying load current. Despite the switch-mode operation of power-conversion systems, the analysis is simplified when high carrier-frequency ratios are used because time-average effects are more easily approximated.

**CONCLUSIONS**

The data presented in Figs 8 to 10 and Table 1 is not meant primarily for device comparison, since some aspects of device performance are not well specified and variability exists in the way in which device performance is specified. The intention has been to demonstrate that usable device current varies with modulating signal frequency [Fig 9b], switching frequency [Fig 10], and the level of soft switching employed [c.f. Figs 9a and 9b]. Predicting usable current does not only require knowledge of device conduction and switching loss but also device thermal conditions, such as thermal impedance, equivalent power pulses for steady-state operation, and in the case of transient load change thermal response to power waveform transients. With wide variation in power-electronics system input and output quantities and modulating and switching frequency possible [eg. VVVF inverters employing hysteresis current control] determining usable current in the presence of tolerance in device characteristics and operating conditions is a complex matter. Temperature-regulated active current limiting would considerably ease this by ensuring that power-stages are always usable up to their full capability under transient, as well as steady-state, conditions.

**REFERENCES**


Appendix-1

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Table-2: Device conduction and switching loss coefficients extracted from data sheets