V A-3

MINIMISING SNUBBERS FOR HIGH-CURRENT EMITTER-SWITCHED TRANSISTORS

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ABSTRACT

High-power emitter-switched transistors have been operated at 20 kHz and 80 A off 600 V, using voltage clamps instead of shunt snubbers. Series snubbing then becomes the dominant source of switching related power-loss and transistor dead-time. An analysis of series snubbers reveals configurations conducive to minimal reset-time and power-loss. Cascode switches operating at high-current ideally require adaptive voltage-clamps which clip at current-dependent voltage levels. Practical realisations of such clamps are given.

INTRODUCTION

Emitter-switching high-voltage power transistors permits safe turn-off with reverse base-current equal to or greater than the collector current. Consequently, lower storage and crossover times are possible than with base-switched transistors, and the dispersion in turn-off performance arising from production tolerance in characteristics and variance in operating junction-temperature is reduced, because high reverse base-current rather than minority-carrier recombination predominates in removing stored charge [1]. Emitter switching is also reported to extend the RBSOA up to the Vcbo rating, effectively giving an increase in Vceo rating with no loss in hfeIc product: normally a higher Vceo rating is achieved at the expense of hfeIc product [2] which is proportional to Vceo exp(-2.3). These benefits have generally been observed and applied to low-current transistors operating at or below 20 A. However, high-voltage, 20 A transistor performance has recently been improved [2,3] using planar fabrication technology more akin to that of MOSFETs which enables more precise semiconductor processing and the fabrication of finer emitter geometries and structures. These devices are reported to be characterised by reduced dispersion in specifications between devices, enhanced RBSOA by greater uniformity of current density over the die area, and reduced storage and crossover times from increased accessibility to stored charge. It therefore seems that at the 20 A current-level most of the emitter-switch benefits have been eroded if not eclipsed and the disadvantage of the cascode, increased drive complexity, higher on-state losses, and sparse history of application, weigh less favourably in comparison. In contrast, large-area transistors (> 10 x 10 mm) constructed using power-thyristor fabrication and packaging techniques, with Vceo and Ic ratings of 1000 V, 300 A and 700 V, 450 A at 150 C [5] are less likely to be superceeded by parallel-connected, highly interdigitated planar transistors (the reasoning is similar as that for MOSFETs). When emitter switched with parallel-connected 50 V MOSFET's, large-area transistors are suited to high-frequency (20-50 kHz) power conversion at medium-power levels above 50kW. A start to the commercial exploitation of high-current emitter-switched transistors has been made [6] with the launch of an isolated power-hybrid, comprising 2 split 1000 V, 100 A cascode switches with inverse-parallel diodes. Like base-switched transistors, optimum cascode-switch performance is dependent on the method of base-current control in the forward direction. Emitter switching does not eliminate the need for the profiled current-source, normally used in low-gain single-transistor operation, and offer the user a voltage-control input. The optimum drive of high-current cascode switches has been investigated [7]. This paper presents the switching waveforms obtained during switching 80 A from 600 V at 20 kHz, the turn-off protection networks employed, and their contribution to net power-loss; and contrasts this with the remaining high series-snubber power-loss. Linear series-snubbers and voltage-clamp based reset circuits are analysed to determine which generates the least power-loss and transistor dead-time. Also, methods of improving supply-referenced voltage clamps, which uphold the transistors Vceo rating at high collector-current, are analysed.

CASCODE SWITCH CIRCUIT

Cascode-switch performance has been observed with circuit fig.1. Series snubber Ls sets turn-on di/dt; soft voltage-clamp Dc, Cc and Rc, holds turn-off Vce below Vceo. Rs operated with Cs, damps the resonant circuit, comprising transistor output capacitance, clamp-loop stray inductance and Cc; and Cm prevents MOSFET avalanching during emitter/base current-commutation and collector-voltage rise. Secondary effects of Cm and Cs, Rs are the aiding of base-emitter junction cut-off, at the start of storage-time and during collector-voltage rise. Fig.2 gives turn-off measurements for a MEDL DT47-1050 transistor operating in Fig.1. Turn-off crossover-time is approximately 130nS for k = 1 (ie. Vce = 1 to 1.3 V) and 100ns for k = 2 (ie. Vce = 1.2 to 1.5 V). Transistor output capacitance (approx. 2.0nF above 400V)

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causes an increase in trv at low-current. The transistor is held out of saturation by a shunt-regulator anti-saturation circuit which only requires connection of a 1 A, 1000 V diode to the collector; thereby preventing diode reverse-recovery influencing transistor turn-off.

CASCODE SWITCH WAVEFORMS

Cascode-switch operation is shown in fig.3 to 8. Features of these are described briefly before analysis of their implications to circuit design. The reverse base-current during storage-time, fig.5, comprises components of collector and reverse emitter current. Early in the storage-time, after Ib reaches Ic, Cm is discharged by the recovery of the emitter junction and produces the current peak. A later effect is avalanching of the emitter junction, at approximately 15 V by stray base-clamp loop-inductance (40nH) which is manifested as a linear fall in base-current after the collector-current fall. Base-clamp loop inductance also controls the initial rate-of-rise of reverse base-current. Fig.3 gives the expanded current-fall and voltage-rise at turn-off. Collector-base junction recovery is virtually complete at 350 V and the subsequent voltage rise is controlled by transistor output-capacitance and Rs, Cs. Fig.6 shows the improvement in storage and crossover time given by an antisaturation circuit. Here both waveforms are triggered by the emitter-MOSFET turn-off edge, 100ns into the trace. The effect of the antisaturation circuit on Vce and its response are shown in fig.4. Fig.7 gives the turn-off waveforms at 80 A, but waveform pairs are not synchronised. Fig.6 and 7 also show the poorer performance of the voltage clamp at higher di/dt, 2000-4500 A/us. Two parasitic effects contribute to initial voltage-overshoot: clamp-diode forward recovery and voltage-clamp loop stray-inductance. Overshoot in fig.6 is largely due to the diode forward-recovery effect. At twice the di/dt, fig.6b, Vfr has increased, but the high-frequency oscillation shows that stray clamp-inductance is dropping a higher voltage to excite its associated resonant circuit. At higher di/dt, fig.7, the stray-inductance component of overshoot is more pronounced. However, clamp-diode forward-recovery remains discernable as an exponentially decaying voltage component (tfr = 200ns). Transistor desaturation (60V) is evident at turn-on in fig.8, during the current-rise. Freewheel-diode reverse-recovery current is 50 A for an 80 A forward current: di/dt was 200A/us. Finally series-snubber reset into the voltage-clamp is seen in fig.8.

SWITCHING POWER-LOSS

The main component of turn-off power-loss is produced by current-voltage crossover. The non-linear voltage waveform is assumed to approximate an exponential in the derivation of [1].

$$P_{off} = E_{dc}\, I_1\, f \left(\frac{t_{rv}}{2.2} + \frac{t_{fi}}{1.6} \right) \qquad (1)$$

trv and tfi are measured between 10% points. Extrapolating the curves of fig.2 allows turn-off power-loss estimation for 100 A, 20kHz and 600 V operation, as 63 W. Turn-off time measurements were made at 21 C. The increase with temperature requires investigation. However, with base-switched large-area transistors, factors of 2 to 3.5 have been obtained [10] between 25 and 150 C. Even if a worst-case loss of 200 W is assumed, this energy is 2.5 to 5 times down on the series-snubber reset-energy, fig.9. A 100 A 3-phase cascode-switch inverter with 5uH snubbers would have snubber-reset losses of 750W and turn-off switching losses between 126 and 400W at low fundamental output-frequencies. Improvement in power-conversion efficiency would result from energy recovery of trapped series-snubber energy. However, in this paper only an analysis of series-snubber configurations is performed to minimise trapped energy, and to identify other criteria for series-snubber selection.

SERIES SNUBBER COMPARISON

High-voltage transistors suffer from delay in moving from linear operation to hard saturation which is manifested by a higher on-state voltage-tail after voltage-fall. Large area high-voltage transistors additionally have a lateral charge-spreading time, akin to thyristors. Therefore, even without reverse-recovery charge in freewheel-diodes, series snubbers would be essential, to prevent severe desaturation up to the dc-rail at turn-on, when the transistor area undergoing conduction would be ill-defined. In overcoming this, accepting a higher di/dt during load current increase than during diode recovery in principle offers a saving in stored energy. For example:
Peak transistor collector-current, Ip = 175 A
Continuous collector-current used, Ic = 100 A
So, peak diode-reverse-current, Irm < 75 A
From fig.9 ,diode reverse di/dt < 110A/us
Maximum transistor di/dt capability is 200 A/us. Therefore, if transistor di/dt up to Ic and diode di/dt during Irm are set independently by Lt and Ld, significantly less reset energy is obtained.

$$\frac{W_{independent}}{W_{same}} = \frac{1 - (1 - k)\, I_o^2}{I_o^2 + I_{rm}^2} \qquad (2)$$

For k=1/2 and di/dt=200A/us, Wind/Wsame = 0.336, and reset energy is reduced from 700 to 302W for a phase-leg operating at 100 A without energy recovery. This principle is difficult to realise simply in practice. The following analysis is of more common series snubbers shown in fig.12. An insight into their operational differences is obtained by examining energy transfer into ideal voltage-clamps. DC-rail current, Idc; load voltage, Vo; and transistor current, Io, are given in fig.12. Energy change in the dc-rail and load are determined from current and voltage waveforms alone. The other parameter of the instantaneous power equation, Edc or Io, is assumed constant. Without diode reverse-recovery charge, waveform fig.12F would result. Diode-recovery delays connection of the load across the dc-rail. However, except in 12C, the voltage-time integrals are all equal by time t6. 12C is different because a proportion of the Io.Irm.L component of energy, stored in L at t3, is dissipated in the transistor and diode. A longer reset-time of Irm-associated energy is also obtained with 12C. At high-current the recovery current would not fully reset during the on-time. Complete reset of the residual Irm and Io would occur in the voltage clamp at transistor turn-off. These disadvantages render 12C unsuitable for high-frequency operation. By forming an asymmetric half-bridge with it and adding inductor, Lst, circuit 12E is obtained. 12E is the only configuration shown with added shoot-through protection. It is applicable to all circuits except 12D. Two additional voltage clamps per phase-leg, as shown in 12E, are required in 12A(a) and 12C. Shoot-through protection does not affect either Irm or Io reset energies or times. It appears, at this stage, that 12C is the only configuration which has undesirable energy-reset properties. A better Irm reset energy and time result in the rest. Other aspects of operation are now examined. A prerequisite of fast high-current switching with minimal snubbing is a very compact physical arrangement, especially of the transistor and voltage clamp, but also of freewheel-diode and voltage clamp if additional local clamps are to be avoided. The main function of the voltage clamp is to hold turn-off Vce below Vceo, under all operating conditions. Being able to use the voltage-clamp to clip the diode voltage at the peak of reverse-recovery and to reset the series snubber, or to take series-snubber energy until a bulk reset-circuit begins to act, are added benefits. Series-snubber circuits 12A(b) and 12B may be eliminated. In each, the voltage-clamp operates in series with a freewheel-diode, giving 2 series forward-recovery effects at the onset of clamp operation. Also, obtaining a low transistor/voltage-clamp loop-inductance would be difficult, particularly in all phase-legs of 12A(b). The transistors, freewheel-diodes and voltage clamps of 12A(a), D(a) and D(b) are connected directly to each other, giving good transistor protection. The disadvantage of 12E is the additional voltage-clamps, although these are required in 12A(a) & D with shoot-through protection. One possible disadvantage of 12A(a) is the parallel operation of voltage clamps. Three voltage-clamps always act in parallel when absorbing Irm or Io related energy. This may be desirable during a fault condition, but it demands close matching of effective clamp-impedance seen by L, to prevent ringing between clamps and excessive power-loss by the clamp nearest L. The advantage in 12A of having a single series-snubber is therefore outweighed. In 12D the phase-leg inductor must reset in the local voltage-clamps. The optimum configuration for high-frequency power-conversion becomes 12D, if shoot-through protection is not required, and 12E if it is. However 12A(a) is worthy of further investigation with and without shoot-through protection to determine if good parallel clamp operation is achievable.

VOLTAGE CLAMP

In the absence of shunt snubbers, fast and hard voltage-clamps are vital. With increasing di/dt and collector current, hard clamping at Edc is increasingly difficult to achieve, cf. fig 6 & 7, despite careful fast-recovery diode selection and close placement of clamp and transistor, Lc<50nH. The high rate-of-change of current, 3000A/us, at current-fall produces a 100 to 180V overshoot above Edc due to clamp loop-inductance and diode forward-recovery. Voltage-overshoot increases average (equ.3) and instantaneous turn-off power-loss, by 11 and 17% per 100V, but the main danger comes from the reduced margin between Vceo

$$P_{toff} = (E_{dc}\, I_1\, t_f \;\; (1 + \frac{2\,k}{n} \;\;) \;\;)/1.6 \qquad (3)$$

and maximum over-shoot. It becomes necessary for reliable high-current transistor operation, to lower the knee of the voltage-clamp below Edc, to compensate for initial clamp-overshoot. A reduced voltage droop is obtained with discharge circuits, designed to minimise discharge energy and give a voltage droop proportional to current. Fig.10 gives 2 circuits for this. Voltage droops on the clamp capacitor are most efficiently produced by discharging to Edc rather than 0V. The ratios of power dissipation and examples are given, where k = (Edc - Vinitial) / Edc .

$$P_{ov}/\,P_{dc} = (2/k - 1) \qquad (4)$$

V_{init}	k	$P_{ov}/\,P_{dc}$
0	1.0	1
300	0.5	3
450	0.25	7

For a 300V droop below Edc, 1/3 of the 0V-rail discharge power loss results from discharging to the Edc-rail. Providing a voltage droop related to current, further reduces clamp-capacitor related power-loss; and may be used because current fall-time generally increases slowly with increasing current. Consequently di/dt increases at higher current. Voltage overshoot is therefore related to current. A voltage droop, to compensate for clamp overshoot at maximum collector-current, which reduces proportionately would suffice.

ADAPTABLE VOLTAGE-CLAMPS

Proposed realisations of current-dependent voltage clamps are given in fig.10. 10a provides complete energy recovery to Edc of stored series-snubber energy at transistor turn-off, and also of energy associated with producing a voltage droop. The method of discharging Cc by Tc and Lc is derived from a non-dissipative snubber circuit (10), where Tc and Lc discharge Cc to 0V by connection to Edc/2, produced by connection of Tc to the centre-point of series-connected capacitors shunting the Edc-rail. In its modified form discharge of Cc below Edc is current-dependent. At transistor turn-off Ls rings up Cc. Cc remains charged until transistor turn-on, when Tc switches on and Lc rings Cc down from Edc by a voltage virtually equal to the peak voltage above Edc at turn-off. With a high chopping-to-fundamental frequency ratio, the current next switched off varies little from the past value that set the voltage droop. The maximum working transistor-voltage above Edc limits the magnitude of voltage droop. Cascode-switch low current-fall time and snubber action, after voltage-clamp forward-recovery voltage peak ensures that the maximum working voltage is Vcbo, 200V above Vceo for a DT47-1050 transistor. Not working above its Vceo rating, gives almost unacceptable capacitor values and reset times.

Ic(A)	Ls(uH)	Cc(uF)	Vcs(V)	trs(us)
100	5	5.0	100	7.9
"	"	2.2	150	5.2
"	"	1.3	200	4.0
"	"	0.8	250	3.1

The maximum voltage rise on Cc at the highest collector-current sets Cc and Ls reset-time, and hence the minimum off-time. The maximum current rating of Tc and Lc sets the Cc reset time. The minimum on-time corresponds to the time after current-zero in Lc, when Tc can block a forward voltage. Failure to turn off Tc results in loss of voltage-droop and excess dissipation in Tc. For the lowest dead times a fast thyristor is required. Energy is advantageously returned to Edc at a time when load-current is commutated between freewheel-diode and transistor. Cc then aids local dc-rail decoupling. In phase-legs, Cc is also required to absorb Irm related energy. Tc should be turned on by collector voltage-fall, which occurs at both transistor and diode turn on. A current-related voltage-droop is also produced at diode turn-off to conserve diode voltage rating. Adaptive voltage-clamp Fig.10b dissipates energy related to the Vcc rise above Edc; and also energy associated with voltage droop, less obviously in the Ls clamp. Phase-leg operation is possible. Capacitor Cc must be smaller than in 10a to achieve usable voltage-droop. Operation relies on having an additional circuit for Ls to take bulk reset-energy. Cc Provides voltage clamping at transistor turn-off, potentially from lower voltage than in 10a , until current is established in Ls reset-circuit. Edc is connected across N1-L1, during current rise at transistor turn-on. T1 has a 1:1 turns ratio. An equivalent circuit shows that L1 and Cc constitute a series-resonant circuit in parallel with Ls. Vcc and IL1 rise during series-snubber action. At the freewheel diode-recovery peak, VLs drops and the energy stored in L1 is transferred to Cc and the bulk reset-circuit. The voltage rise on equivalent-circuit Cc translates to a fall in Vc in the actual circuit. By choice of L1, Ls and Cc the voltage droop may be varied to the full Edc. For low values of series-snubber inductance, when current increases almost linearly, Edc is applied to N1 and L1 for a time proportional to current. L1 is required to be 5 to 10 times Ls to prevent significantly reducing the effective series-snubber inductance at transistor turn-on, when L1 operates in parallel with Ls. For the same initial control of di/dt, Ls is increased by k.

Ls = original value of series-snubber
kLs = modified value with L1 in parallel

$$k = L_1 \; / \; (L_1 - L_s) \tag{5}$$

Reset-energy of Ls is therefore increased by k. At turn-on, energy associated with lowering Vcc, before freewheel-diode recovery peak, is stored in Ls by virtue of its larger value. At transistor turn-off when stray inductance charges Cc above the Edc, transformer operation is reversed and Cc is discharged into the Ls reset-circuit, providing T1 does not saturate. The equivalent reset-loop of Cc is given in fig.10b. While no additional switches are used in this voltage-droop circuit, another reset-circuit is required for Ls; and to make this non-dissipative would likely require switches. Therefore, the potential to rapidly discharge a small capacitor during current rise. Thereby placing less constraint on minimum on-time, must be weighed against increased circuit complexity, higher trapped-energy at turn-off, more complicated design procedure and greater influence of parasitic effects on voltage-droop magnitude because of the smaller capacitor, when considering use of 10b. In the absence of other methods of discharging Cc to Edc, 10b serves to show the simplicity of 10a.

SOFT VOLTAGE CLAMP DESIGN

In the emitter-switch test circuit, fig.1, a series-snubber is integrated with a soft voltage-clamp, which dissipates energy in a resistor connected to the dc-rail. An analysis of this and other discharge circuits has been conducted for performance comparison, especially of series-snubber reset-time for a given voltage overshoot. Fig.11 shows the integrated series-snubber reset-circuit and soft voltage-clamp with a generalised discharge circuit, Z. The reduction of the clamp to arrive at a manageable equivalent circuit is given in 11b and c. Ls comprises lumped stray and series-snubber inductance. Most of the capacitor discharge circuits considered, fig.13, are permanently connected to the clamp capacitor. However switched discharge circuits are used especially in energy-recovery circuits. Equations for series-snubber current, Is; capacitor-voltage change above Edc, Vc ; and L and C reset times, tri and trv, have been derived for 13A to E. Equations describing capacitor-voltage in 13C to E change at tri. The circuit-model reduces further to a parallel-connected capacitor and resistor in 13C. Hence the exponential voltage fall after tri. Fig.13E is a further simplified equivalent circuit of 13D, devised to give greater insight into the effect of resistor and connection inductance. Fig.13A is included as a yardstick to compare tri. For a given voltage rise above Edc at series-snubber reset, the capacitor value in 13B is easily set for any L. In 13C, both C & R take reset-energy from the instant of transistor turn-off and the equations describing operation do not give a single solution for R and C, once voltage-rise etc are specified. Fig.14 shows the difference made by the Q of the circuit. A critically damped circuit gives long tri and trv reset-times, 14A. An underdamped circuit gives higher trv and di/dt at zero-crossover and shorter tri, 14B. Fig.14D shows Is and Vc for a higher Q, 2.65. The tendency towards a poor compromise between trv and tri is evident. The exponentially decaying capacitor-voltage is seen in 14D. As Q is increased Is zero-crossover and voltage peak, Vcp move closer and the RC time-constant, rapidly increases, RC=L.(Q exp2). zero-crossover di/dt also increases cf.14A to D. Fig.14B gives a good compromise. Q of 0.866 is selected to give a current-zero to minimise exponential tailing. Fig.14C gives theoretical Is and Vc changes for the components used in the tested cascode-switch circuit, selected empirically. Fig.8 shows the corresponding experimental waveform at 80A and 600V. Vc occurs superimposed on Edc in the actual circuit. The initial voltage-spike at transistor turn-off is due to voltage-clamp forward-recovery. The predicted values for clamp-capacitor voltage-peak, Vcp and tcp of 58V and 2us agree with waveform values. Using the components of 14B, with optimum Q, would give a Vcp=90V and tri=4us. To compare component values and tri for different turn on di/dt, a Q of 0.866 was used to calculate R and C values for 13C. The R and C values, and C values for 13B are plotted in fig.15A. The parallel connection of R & C in 13C significantly reduces the capacitor value required. Generally C13C=C13B/5. Energy recovery circuits may therefore require 5 times the capacitance of the optimised dissipative circuit. tri for 13A,B and C are given in fig.15B for a range of di/dt values. tri increases inversely with di/dt because less series-snubber inductance is required at high di/dt. 13A gives the smallest tri value as expected. 13C values are 21% higher, and 13B are 57% higher. Translating tri values of 13C into maximum average output-voltage for a chopper subject to minimum off-time imposed by tri gives fig.15C. The curves of fig.15 enable comparison of voltage-clamp discharge circuits, and show the nature of change in parameters versus series-snubber inductance. Snubber inductance is thus seen to limit conversion-efficiency and minimum on and off times, and therefore maximum average output-voltage or maximum switching frequency.

CONCLUSIONS

a) Series snubber power-loss dominates in high-frequency phase-legs with switches capable of square load-line turn-off. Power-loss from the reset of trapped-energy cannot be significantly reduced by choice of series-snubber circuit. Based on other criteria some series snubbers are better suited to high-frequency power-conversion.

b) Capacitor-based voltage-clamps may be precisely designed to satisfy a given peak-voltage and inductor reset-time. An optimum Q near 0.866 has been identified for the commonly used voltage-clamp, with a discharge resistor to Edc.

c) Emitter-switched transistors require adaptable voltage clamps to hold collector-voltage below Vceo at high current without impracticable layout, or complex compensated voltage-clamps. Emitter switching gives low current-fall at turn off. The resulting overshoot on the transistor collector is difficult to clamp given the forward-recovery time of simple practical voltage clamps.

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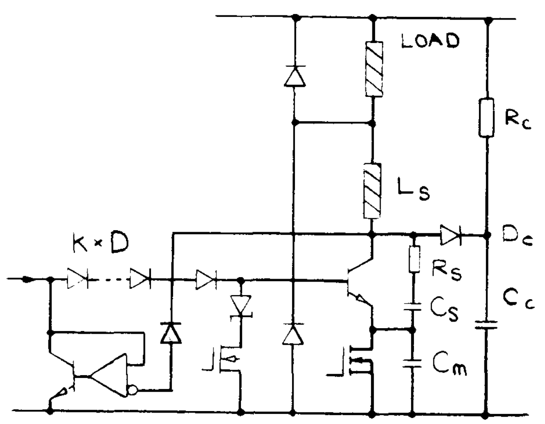

FIG.1 CASCODE SWITCH CIRCUIT

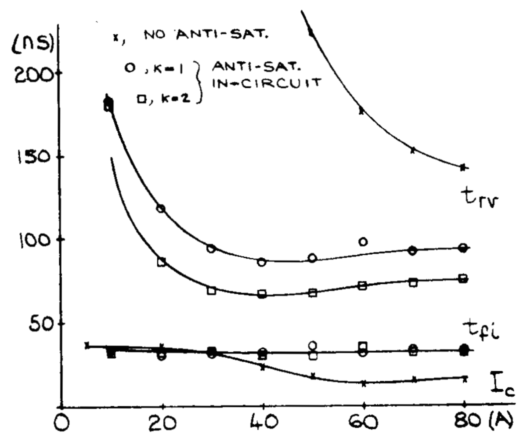

FIG.2 VARIATION IN VOLTAGE RISE & CURRENT FALL TIME WITH COLLECTOR CURRENT,@600V

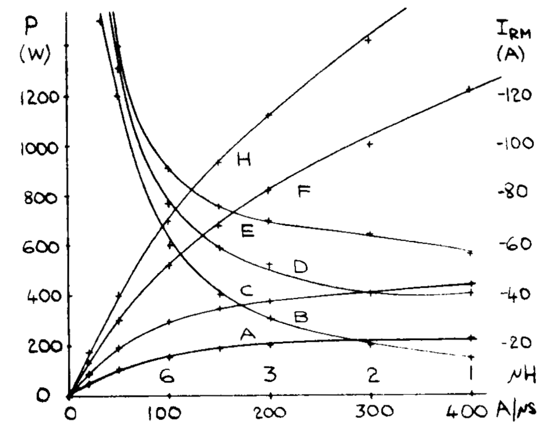

FIG.9 POWER-LOSS FROM Io & Irm-RELATED SERIES-SNUBBER TRAPPED ENERGY & PEAK REVERSE FREEWHEEL DIODE CURRENT V. TURN-ON di/dt

A Prm(typ)
B Prm(max)
C Prio
D Ptotal(typ)
E Ptotal(max)
F Irm(typ)
H Irm(max)

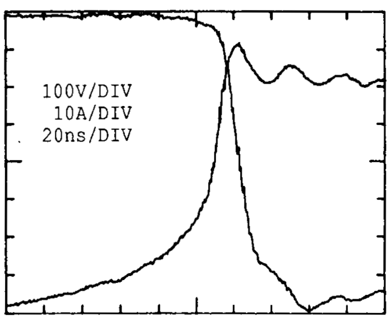

FIG.3 VOLTAGE RISE & CURRENT FALL (INDIRECTLY AS CURRENT IN CLAMP DIODE),@80A&600V

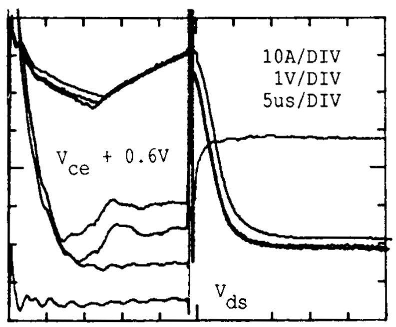

FIG.4 TRANSISTOR AND EMITTER MOSFET ON-STATE VOLTAGE AND SERIES-SNUBBER CURRENT, AT DIFFERENT SATURATION LEVELS

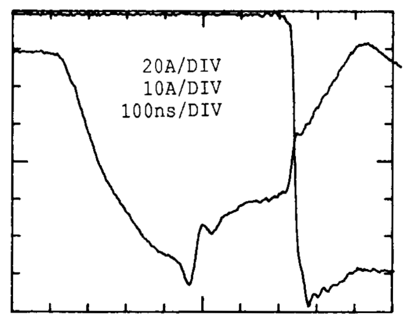

FIG.5 REVERSE BASE-CURRENT DURING STORAGE AND CURRENT FALL TIME,@80A&600V

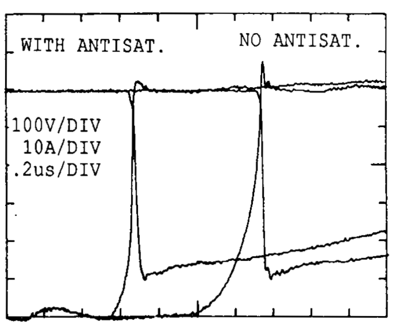

FIG.6 COLLECTOR VOLTAGE RISE & CURRENT FALL WITH AND WITH OUT ANTI-SATURATION,@50A&600V

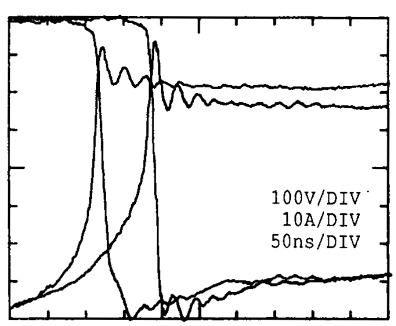

FIG.7 COLLECTOR VOLTAGE RISE & CURRENT FALL WITH AND WITH OUT ANTI-SATURATION,@80A&600V

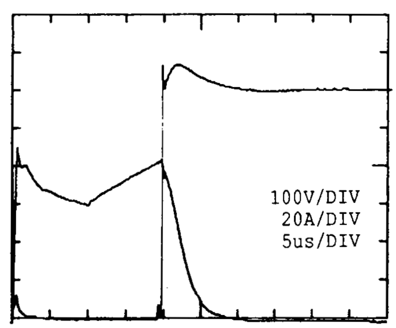

FIG.8 SERIES SNUBBER CURRENT AND COLLECTOR VOLTAGE OVER COMPLETE SWITCHING-CYCLE

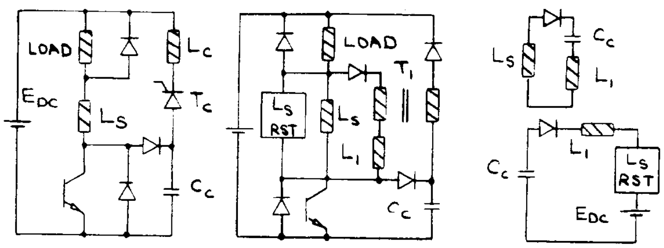

FIG.10 ADAPTIVE SOFT VOLTAGE-CLAMPS

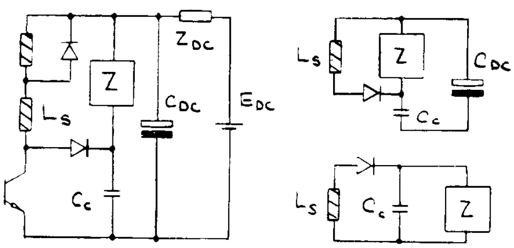

FIG.11 REDUCTION OF GENERALISED SOFT VOLTAGE-CLAMP

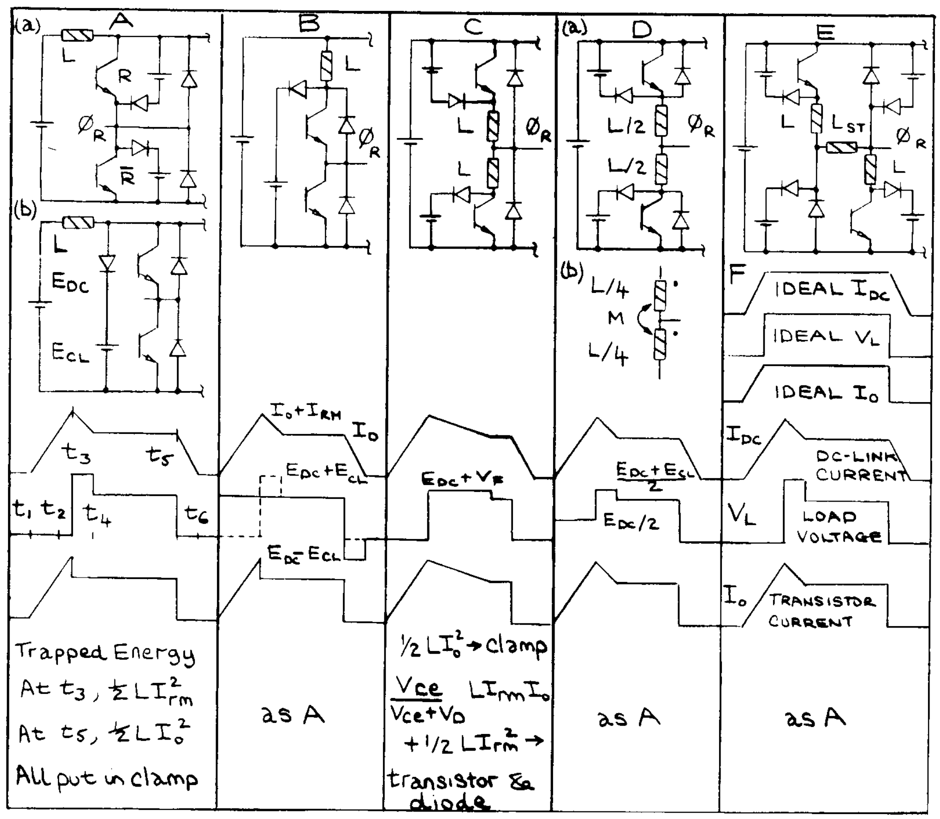

FIG.12 SERIES-SNUBBER CONFIGURATIONS & WAVEFORMS TO ILLUSTRATE ENERGY TRANSFER IN A SWITCHING CYCLE

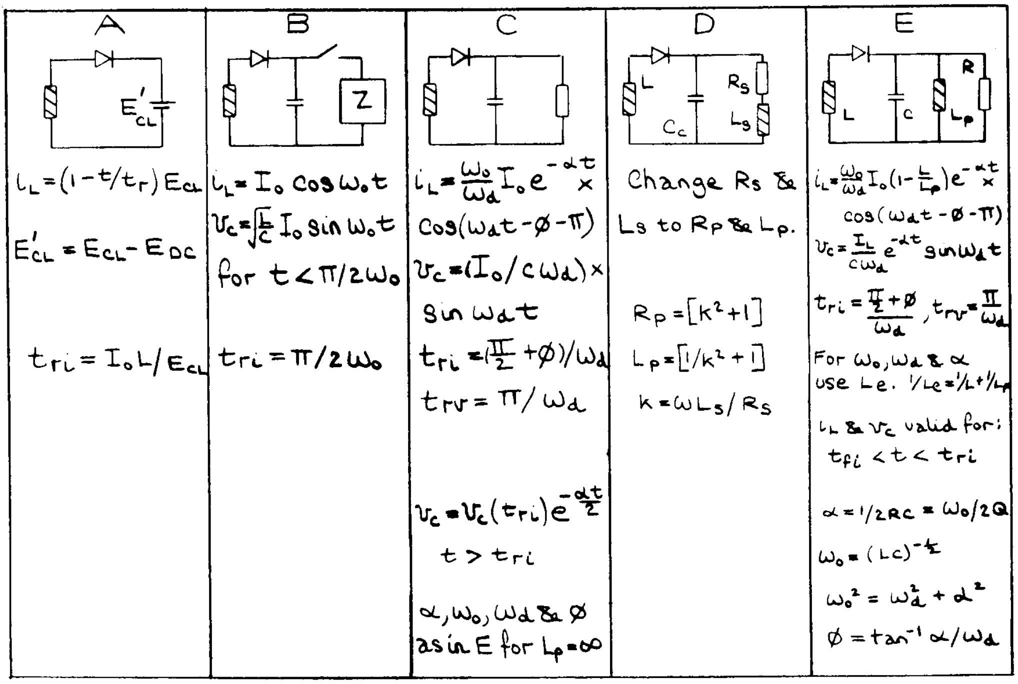

FIG.13 MODELS OF VOLTAGE-CLAMP RESET-CIRCUITS

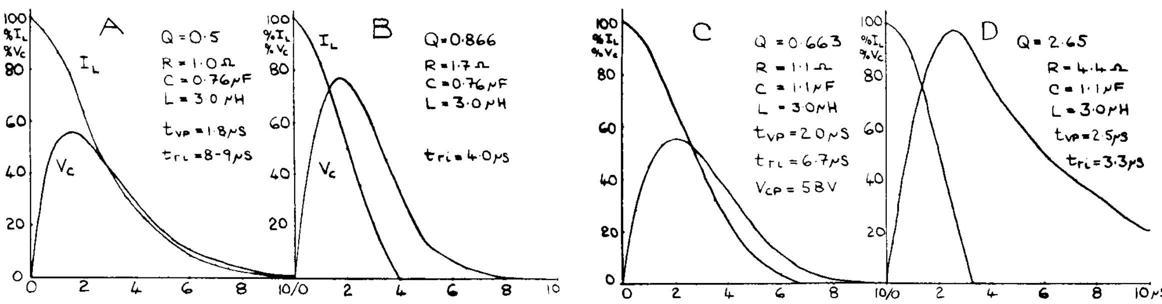

FIG.14 THEORETICAL SERIES-SNUBBER RESET-CURRENT & VOLTAGE-CLAMP WAVEFORMS FOR DIFFERENT CIRCUIT Q

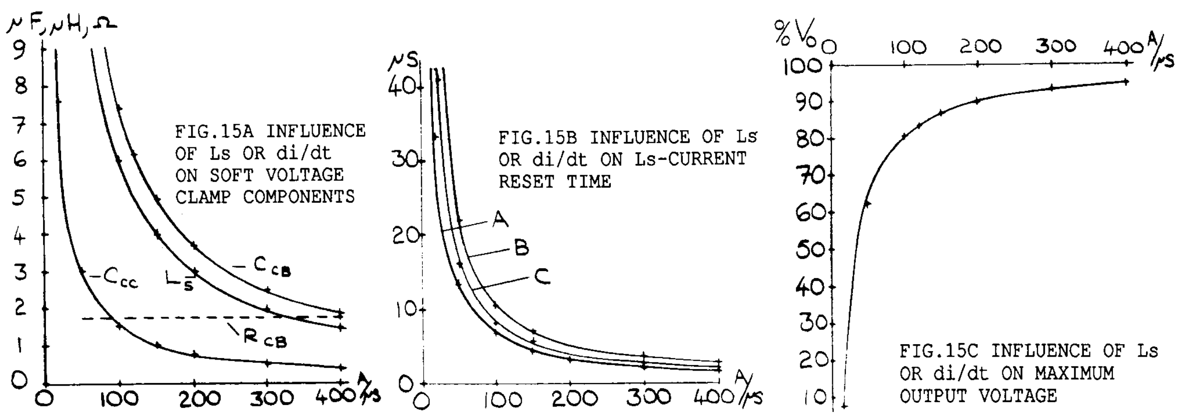

FIG.15A INFLUENCE OF Ls OR di/dt ON SOFT VOLTAGE CLAMP COMPONENTS

FIG.15B INFLUENCE OF Ls OR di/dt ON Ls-CURRENT RESET TIME

FIG.15C INFLUENCE OF Ls OR di/dt ON MAXIMUM OUTPUT VOLTAGE