High frequency protection scheme for multi-terminal HVDC overhead lines

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Abstract

This paper proposes a novel protective relaying technique for multi-terminal HVDC system based on the high frequency components in the current signals received at each end of the DC transmission line. A simple model of a mono-pole, ground return, MTDC system is built in ATP draw using a distributed parameter, frequency dependent overhead line model. For this system, the high frequency content in the current signal directly following a fault (at approximately 0.2 kHz) is shown to vary significantly with fault location but not fault resistance. The protection algorithm is then validated in real time using an RTDS system, where both the ATP primary system model and the MATLAB developed algorithm are demonstrated in a real time context.

1 Introduction

Recent developments in DC circuit breakers and VSC based converters mean that multi-terminal HVDC is becoming increasingly technically and economically feasible. Multi-terminal HVDC (MTDC) has recently been proposed for connecting a large number of offshore wind farms or as a means to transfer solar power from Saharan Africa to major European load centres. It is therefore vital that adequate protection algorithms are developed for such systems.

Conventional protections for HVDC point to point links are travelling wave and voltage derivative with undervoltage and differential protection usually deployed as backup protection [1]. These methods all have various advantages and disadvantages. For example, both voltage derivative and travelling wave protection are based on detection of the initial wave front following a disturbance. This makes them extremely fast, yet beyond a certain threshold, high fault loop impedances will render detection difficult due to the damping of the waves [2]. Differential protection offers high accuracy and simplicity and is therefore quite reliable, but it requires a telecommunications link between the terminals. Undervoltage is effective at detecting high impedance and remote faults that do not trip the main protection and so is often used as secondary or backup protection. Simple overcurrent may also be used on shorter systems, but its application is limited since it does not provide fault location. Impedance based distance protection is limited to one dimension since there is no pre-fault reactance to measure on a DC line. Variations in fault resistance therefore lead to large errors in distance protection, and it is seldom used without considerable augmentation.

The multi-terminal case introduces an extra layer of complexity into an HVDC system. Following a short circuit fault on a multi-terminal system, large currents will flow on all parts of the system from the converter stations to the fault point, potentially reversing the pre-fault current and power flow in some lines. This sudden change of power flow may cause wider problems on the connected AC system as well as the DC system, so it is vital that the faulted zone is de-energised as quickly as possible, without loss of the healthy parts of the system.

It is important that protection engineers have a number of options and combinations of protection for MTDC systems so that they may hedge the various advantages and eliminate short-comings of individual methods against each other.

One possible method of augmenting existing protections is use of high frequency information generated following a fault. This is different to conventional travelling wave protection since it uses more of the voltage or current time series than just the initial fault wave-front. This paper describes such a method.

The rest of the paper is organised as follows. Sections 2 and 3 describe the ATP test system. Section 4 describes the algorithm. Sections 5 and 6 describe the RTDS simulation and results and Section 6 draws conclusions and suggests further work.

2 Test system

Large real-world MTDC systems are rare, with only two significant multi-terminal systems existing as of 2012. This paper therefore uses the system proposed in [3] as a test system. This is a four-terminal 500 kV mono-pole ground return HVDC system from California to Wyoming via Utah and Nevada. Its topology is shown in figure 1. Under normal operation rectifier 1 and 2 feed inverter 3 and 4 via HVDC lines 1 2 and 3, which are 650 km 530 km and 370 km in length respectively.

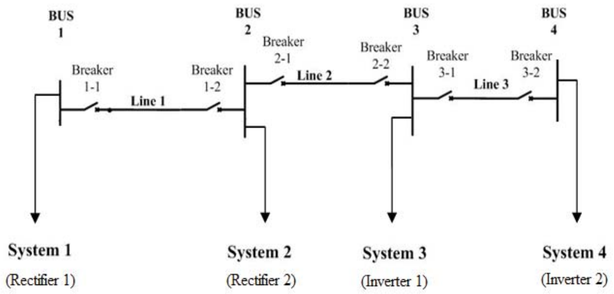

Figure 1: The four terminal DC test system used in this paper

A model of this system was built in ATP-draw. The rectifiers and the inverters were modelled as ideal 500 kV DC voltage sources behind an impedance to simulate the short-circuit capacity at that point in the system. Although in practice, the post fault behaviour will be heavily influenced by the power electronics in the converters and their control loops, this simplification was made since it allows for isolated study of high frequency transients present in DC overhead lines. It is also somewhat justified since following a fault, all the converter stations will act like rectifiers, feeding the short circuit. The effect of detailed modelling of the converter stations on this protection technique will be investigated later publications.

The transmission line was a mono-pole ground return assembly modelled as a single phase line using the J-Marti model in ATP-draw. Reference [4] demonstrates the importance of a frequency dependent line model in HVDC line protection studies. All lines were assumed to have the same parameters, with the only variation being length. Full detailed system parameters are included in the appendix. Extensive short circuit fault studies were conducted on this test system. This involved splitting one line into separate subsections and grounding the line with a switch through a purely resistive fixed fault impedance. The ATP draw test system can be seen in figure 2.

3 Preliminary Studies

Short circuit studies were conducted at various line locations and with various fault resistances on line 1. These were at 10%, 20%, 50%, 80% and 90% of the line length and with fault resistances of 0 Ω 2 Ω, 10 Ω, 20 Ω, 50 Ω and 100 Ω

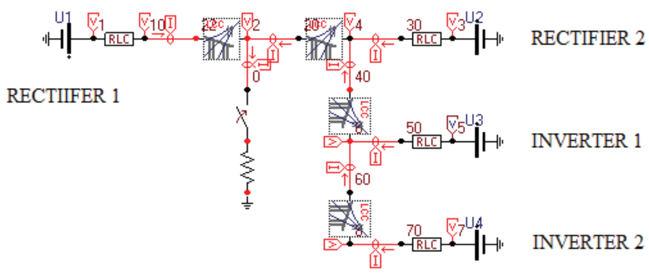

Figure 2: ATP-draw test model canvas

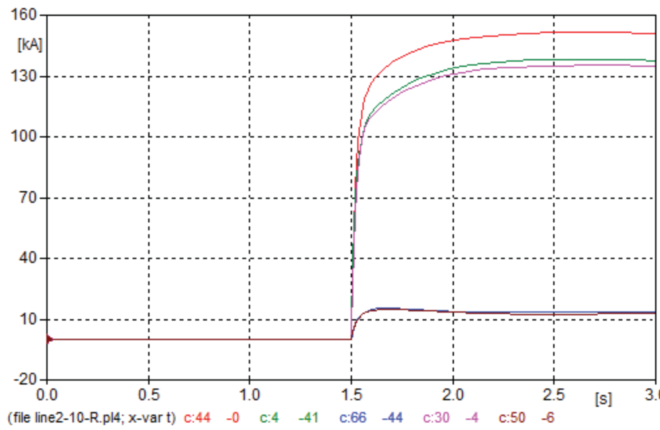

Figure 3: Time series of fault currents measured at different buses on the system. Fault occurs at 1.5 s. Highest currents are measured at buses nearest the short circuit.

Studies showed that the fault current decreases at an increasing distance away from the fault point. This is due to the increasing resistance between the measuring point and the fault. The relative fault current level at different buses can be used to determine on which line the fault exists. Since the *relative* levels are independent of fault resistance this is robust to variations in this parameter.

The current signals were decomposed into their time-dependent constituent frequencies using the short-time Fourier transform and analysed. The Discrete Fourier Transform is described by (1)

$$y_{p+1} = \sum_{j=0}^{n-1} (e^{-2\Pi i/n})^{jp} x_{j+1} \qquad (1)$$

Where p is the index of the vector y and j is the index of vector x. Both p and j run from 0 to n-1. If x is a continuously sampled discrete time series or space vector, y is defined as the frequencies within such a signal between DC and the sampling rate Fs. In the Short time Fourier transform (STFT) the original time series is windowed and then subjected to the DFT. The windowing function used in this work was the Hann window, described by (2)

$$\omega(n) = 0.5\left(1 - \cos\left(\frac{2\pi n}{N-1}\right)\right) \quad 1 \le n \le N \quad (2)$$

This process was repeated once per sample with the windowing function being moved one sample further in the time series for each successive sample. This process yields a three dimensional signal which varies with magnitude in both frequency and time. The ATP simulation step size was $1\text{x}10^{-5}$ s corresponding to a sampling frequency, Fs, of 100 kHz. This was then exported to MATLAB and down sampled by a factor of one hundred to 1 kHz. The window length was 64 samples yielding 64 frequency bands 15.63 Hz wide.

Extensive studies showed that for this system, the magnitude of frequency band 13, located at 189 - 203 Hz, varied significantly with location but not with fault resistance. Figure 4 shows how fault impedance affected the frequencies at a fault location on line 1 at 10% distance from rectifier 1. It can be seen that only at 50 Ω and 100 Ω the magnitude is significantly attenuated by approximately 22% and 40% respectively.

In contrast, figure 5 shows how the magnitude of the 13th frequency band varied with fault distance at fixed fault impedance of 2 Ω. Measurements were made at each end of line 1. The relationship of the magnitude with fault distance is non-linear. The peak magnitudes of this frequency band were slightly affected by changing fault resistance, but it's proportionality to the magnitude of the current at the opposite bus was not, suggesting that a fault location algorithm could be based on this ratio.

4 Basis of protection algorithm

On the basis of the relationship shown in figure 5, equations (3) and (4) were developed to estimate the fault distance D, in percentage line length from breaker A.

If A>=B:

$$D = \left| \frac{B}{B+A} \right| \times 100 \qquad (3)$$

If B>A

$$D = 1 - \left(\left| \frac{A}{B+A} \right| \times 100 \right) \qquad (4)$$

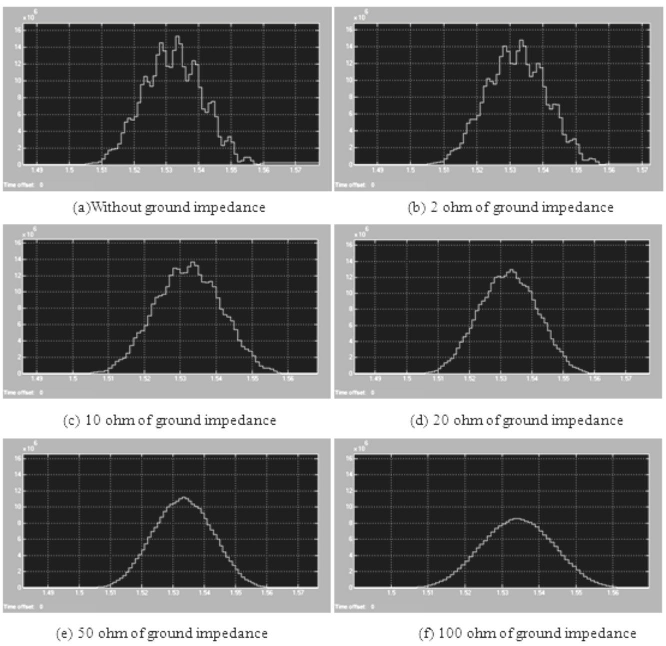

Figure 4: Variation of magnitude of the 189-203 Hz band with fault resistance at 20% of line length

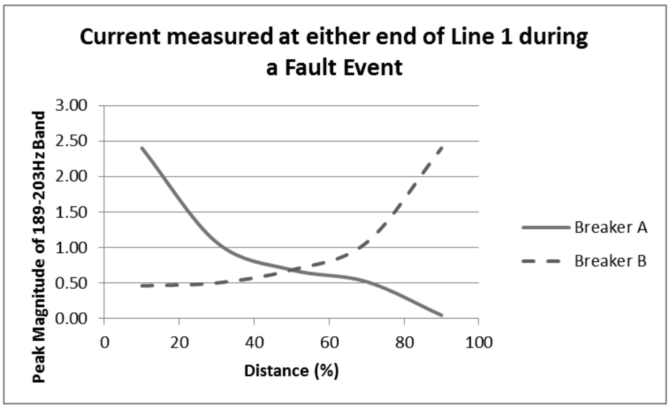

Figure 5: Variation of magnitude of the 189-203 Hz band with fault location on line 1.

Where:
A is the magnitude of the current passing through Breaker A.
B is the magnitude of the current passing through Breaker B.
D is the distance along the line, as a percentage value, the fault occurs.
D corresponds to the location of breaker A. D=100 corresponds to the location of breaker B.

5 Real time implementation

The RTDS is a hardware platform for simulating electric power systems at high bandwidth in real time. The base time step of the simulation is 50 µs, and the manufacturers specify an accuracy of up to 3 kHz. The RTDS can simulate primary and secondary system of arbitrary topology, where the complexity is only limited by the number of processors in the particular RTDS system.

The MTDC test system in section 3 and logic circuits to implement the algorithm in section 4 were built on an RTDS system. Use of the software to harness the RTDS is comprised of two main stages. First, the user designs a power system and secondary system in the DRAFT sub-application. This is then compiled and run in real time in the RUNTIME application. The draft and runtime stages for the MTDC test system are shown in figures 6 and 7 respectively. The protection logic is contained within several subsystems. One simulation run is shown in figure 7. In this case, the algorithm fault location is identified as at 83% of the line length, which is 7 % lower than its true value of 90%. After a brief settling period, the fault location is obtained around 20 ms after the fault inception.

In contrast to the ATP model, the fault model used in the real time simulation was a more realistic primary arc model with only the nominal arc fault resistance specified, to simulate a realistic short circuit line to ground arcing fault. More information about the arc model can be found in [5].

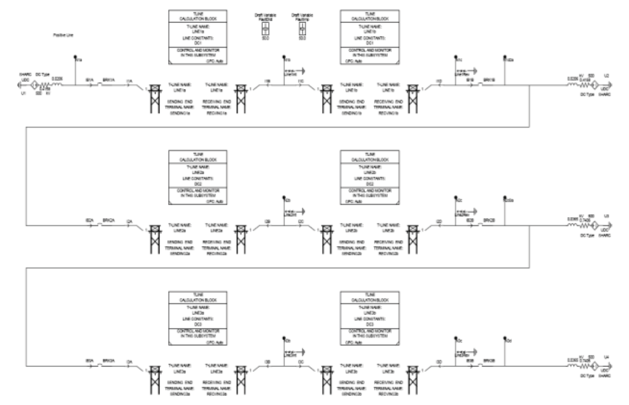

Figure 6: Primary MTDC system model in RSCAD DRAFT program

6 Real time results

The algorithm was tested for five fault locations along line 1, namely 10%, 30%, 50%, 70% and 90% of the line length. Each location was tested for six nominal fault resistances of 0.1 Ω, 1 Ω, 2 Ω, 10 Ω, 20 Ω, 50 Ω and 100 Ω. Each set of fault conditions was tested three times. Results are presented in Table 1.

It can be seen that the average error in the algorithm is always less than approximately 10% for all fault impedances, and for the majority of the fault resistances less than 5%. The algorithm performs less well in the centre of the line and at high fault resistances. This is identified as an area for further improvement.

7 Conclusion

A fault location based protection scheme for a MTDC system has been researched in ATP-draw and validated in real time using an RTDS. Further work is required to improve the accuracy of the algorithm and to determine its robustness for different system topologies and in the presence of accurate models of the converter stations.

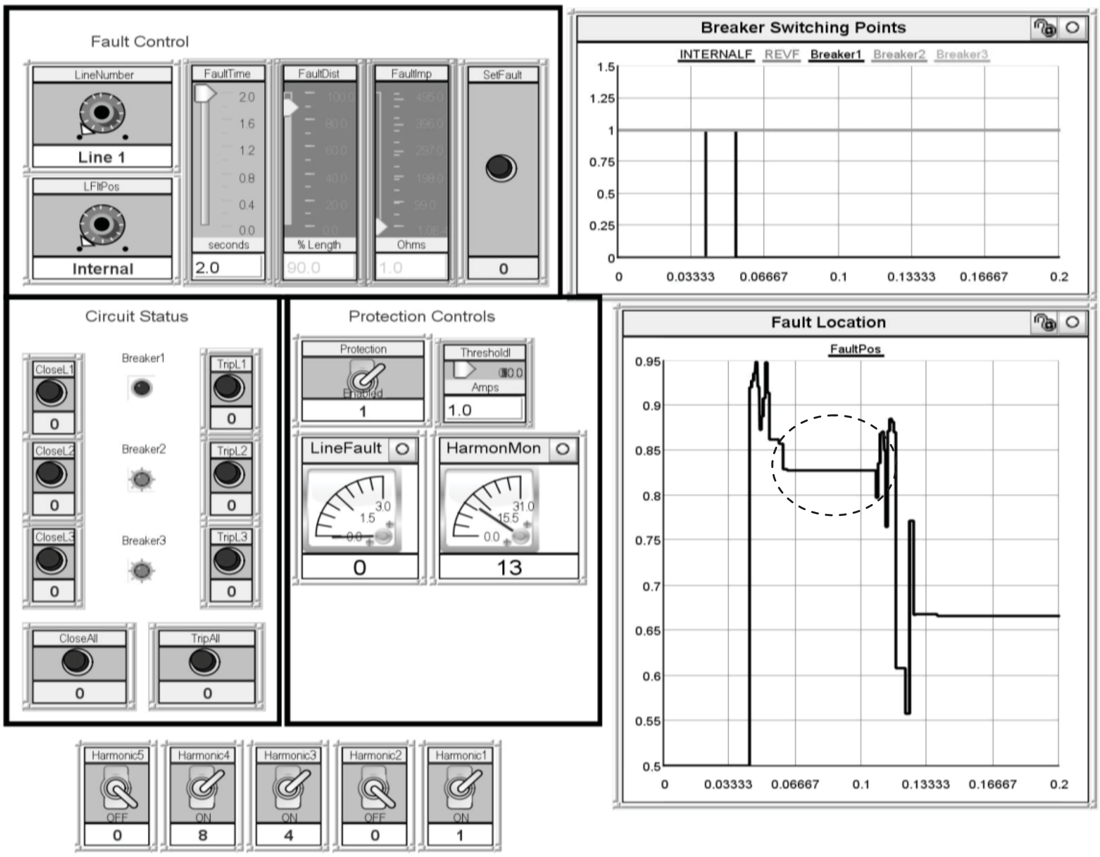

Figure 7: RSCAD RUNTIME canvas: in this case, with the fault set to 90% line length, the algorithm identifies the fault to be around 83% of the line length when the output has time to settle after about 20 ms, and is marked on the "Fault Location" plot.

	Measured Distance											
Actual	0.1 Ω			1 Ω			2 Ω			10 Ω		
	TEST 1	TEST 2	TEST 3	TEST 1	TEST 2	TEST 3	TEST 1	TEST 2	TEST 3	TEST 1	TEST 2	TEST 3
10%	7.50%	12.50%	6.00%	8.50%	6.00%	11.00%	7.61%	12.80%	11.40%	13.70%	11.40%	12.60%
30%	36.00%	32.50%	35.50%	38.00%	36.00%	34.50%	37.50%	36.30%	40.10%	35.20%	36.80%	36%
50%	52.50%	53.00%	53.00%	57.00%	56.00%	60.00%	60.10%	53.30%	55%	55.80%	57.90%	58.40%
70%	76.00%	67.00%	72.00%	72.00%	70.00%	71.00%	69.20%	73.60%	65.60%	65.30%	70.30%	74.80%
90%	80.00%	83.00%	78.00%	84.00%	81.00%	84.00%	83.50%	85.90%	76.20%	82.90%	77.80%	81.10%

	Measured Distance											
Actual	20 Ω			50 Ω			100 Ω			Actual	Average Error	Standard Deviation
	TEST 1	TEST 2	TEST 3	TEST 1	TEST 2	TEST 3	TEST 1	TEST 2	TEST 3			
10%	5.10%	6.10%	15%	10.10%	8.50%	7.90%	16.40%	16.40%	25.20%	**10%**	**3.59%**	**3.16%**
30%	36.50%	43.70%	36.10%	41.60%	45.40%	55.10%	51%	55.50%	64.30%	**30%**	**11.12%**	**8.48%**
50%	59.20%	59.90%	59.90%	69.70%	62.60%	64.30%	73.90%	74.40%	76.50%	**50%**	**10.59%**	**7.28%**
70%	70.10%	73%	72.10%	72.40%	73.20%	78.50%	86.20%	89.30%	80.10%	**70%**	**4.64%**	**5.09%**
90%	83.10%	86.40%	79.20%	96%	97%	96.90%	97.90%	94.90%	99.80%	**90%**	**7.92%**	**2.72%**

Table 1: Results of the real-time simulation test.

5 Appendix

Attribute	Line 1	Line 2	Line 3
Length (km)	650	530	370
Resistivity (Ω/km)	0.0585	0.0585	0.0585
No. Sub Conductors	2	2	2
Sub conductor Radius (cm)	1.55	1.55	1.55
Sub Conductor Spacing (cm)	45.72	45.72	45.72
Height at Tower (m)	21.34	21.34	21.34
Height at Midspan (m)	10.67	10.67	10.67
Ground Resistivity (Ωm)	58.5	58.5	58.5

Table 2: Overhead line parameters.

	Nominal DC Voltage	500kV
Source Impedance	Rectifiers	R=0.4158ohm, L=0.0206H
	Inverters	R=0.7406ohm, L=0.0365H

Table 3: MTDC system source parameters

Acknowledgements

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