The Transport Properties of Electrons and Holes in a Silicon Quantum Well

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Award date: 2014

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The Transport Properties of Electrons and Holes in a Silicon Quantum Well

submitted by

David Simon Downing Tregurtha

for the degree of Doctor of Philosophy

of the

University of Bath

Department of Physics

February 2014

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Acknowledgments

I am indebted to my PhD supervisor Dr. Kei Takashina for his patience and incredible insight into physics in general. His unceasing curiosity and questioning was invaluable when analysing the data obtained during experiments. I would not be the researcher I am today without his guiding influence.

I would also like to thank Dr. Margaret Hopkins, Dr. Stephen Wedge and Dr. Sivapathasundaram Sivaraya for their invaluable advice in use of the machines and wet etching techniques within the nanofabrication facility at The University of Bath. Additionally, Paul Reddish and Wendy Lambson deserve thanks for their help in creating and obtaining technical items for setting up the laboratory where experiments would be conducted.

The other PhD students and fellow researchers in the Nanoscience group provided many enjoyable social outings, some of which are only vaguely recalled while others are too entirely memorable.

The studious and patient nature of Dr. Akira Fujiwara and Dr. Jinichiro Noborisaka during my time working at the Nippon Telegraph and Telephone Corporation in Japan greatly aided my study there. I would like to thank them for inviting me to work in such an amazing place. I think also my love of sushi substantially aided my time in Japan. I am also sincerely grateful to the other foreign students working there with whom I had a great time - especially our ascent of Fuji - and who helped me when my very basic grasp of Japanese failed.

I am also grateful to Dr. Benjamin Piot and the technical staff at the CNRS in Grenoble for their collaboration and support in using their experimental apparatus.

Finally, but by no means least, I would like to thank my family for their continued support - especially my parents; my Mother for sparking a lasting interest in physics from a young age and my Father for his constant questioning and proof-reading of my thesis.
Published Work

The author of this thesis is a named author on the following papers:


# List of Abbreviations

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>2D</td>
<td>Two-dimensional</td>
</tr>
<tr>
<td>2DCG</td>
<td>Two-dimensional carrier gas</td>
</tr>
<tr>
<td>2DEG</td>
<td>Two-dimensional electron gas</td>
</tr>
<tr>
<td>2DHG</td>
<td>Two-dimensional hole gas</td>
</tr>
<tr>
<td>( \hbar )</td>
<td>Planck’s constant divided by ( 2\pi )</td>
</tr>
<tr>
<td>( \Delta_V )</td>
<td>Magnitude of the valley splitting</td>
</tr>
<tr>
<td>( \Delta_Z )</td>
<td>Magnitude of the Zeeman splitting</td>
</tr>
<tr>
<td>( \mu_B )</td>
<td>The Bohr magneton</td>
</tr>
<tr>
<td>( \mu_e )</td>
<td>Electron mobility</td>
</tr>
<tr>
<td>( \mu_h )</td>
<td>Hole mobility</td>
</tr>
<tr>
<td>( \sigma )</td>
<td>The Pauli spin matrices</td>
</tr>
<tr>
<td>( \nu )</td>
<td>The filling factor</td>
</tr>
<tr>
<td>( \Psi )</td>
<td>The carrier wavefunction</td>
</tr>
<tr>
<td>( \mathbf{A} )</td>
<td>The magnetic vector potential</td>
</tr>
<tr>
<td>( \mathbf{B} )</td>
<td>The magnetic field vector</td>
</tr>
<tr>
<td>BOX</td>
<td>Buried oxide</td>
</tr>
<tr>
<td>( B_{\text{TOT}} )</td>
<td>The magnitude of ( \mathbf{B} )</td>
</tr>
<tr>
<td>( B_{</td>
<td></td>
</tr>
<tr>
<td>( B_{\perp} )</td>
<td>The magnetic field applied perpendicular to the plane of the 2DCG</td>
</tr>
<tr>
<td>( C_B )</td>
<td>Capacitance between the back gate and the carriers</td>
</tr>
<tr>
<td>( C_{\text{BOX}} )</td>
<td>Geometric capacitance of the buried oxide</td>
</tr>
<tr>
<td>( C_{\text{eh}} )</td>
<td>Geometric capacitance between the electrons and holes</td>
</tr>
<tr>
<td>( C_F )</td>
<td>Capacitance between the front gate and the carriers</td>
</tr>
<tr>
<td>( C_{\text{FOX}} )</td>
<td>Geometric capacitance of the front oxide</td>
</tr>
<tr>
<td>( C_{\text{he}} )</td>
<td>Geometric capacitance between the holes and electrons</td>
</tr>
<tr>
<td>( C_{\text{SOI}} )</td>
<td>Geometric capacitance of the silicon-on-insulator</td>
</tr>
<tr>
<td>( d_{\text{BOX}} )</td>
<td>Nominal thickness of the buried oxide</td>
</tr>
<tr>
<td>( d_{\text{eh}} )</td>
<td>Distance from the 2DEG to the 2DHG</td>
</tr>
<tr>
<td>( d_{\text{FOX}} )</td>
<td>Nominal thickness of the front oxide</td>
</tr>
<tr>
<td>( d_{\text{hc}} )</td>
<td>Distance from the 2DHG to the 2DEG</td>
</tr>
<tr>
<td>Symbol</td>
<td>Definition</td>
</tr>
<tr>
<td>--------</td>
<td>------------</td>
</tr>
<tr>
<td>$d_{\text{SOI}}$</td>
<td>Nominal thickness of the silicon-on-insulator - also the quantum well thickness</td>
</tr>
<tr>
<td>$e$</td>
<td>The electronic charge</td>
</tr>
<tr>
<td>$E(k)_C$</td>
<td>The dispersion relation of the conduction band</td>
</tr>
<tr>
<td>$E(k)_V$</td>
<td>The dispersion relation of the valence band</td>
</tr>
<tr>
<td>FOX</td>
<td>Front oxide</td>
</tr>
<tr>
<td>$g$</td>
<td>The Landé $g$-factor</td>
</tr>
<tr>
<td>$g^*$</td>
<td>The effective Landé $g$-factor</td>
</tr>
<tr>
<td>$G_e$</td>
<td>Differential conductance of the electrons</td>
</tr>
<tr>
<td>$G_h$</td>
<td>Differential conductance of the holes</td>
</tr>
<tr>
<td>$g_{2\text{DDOS}}$</td>
<td>The 2D density of states</td>
</tr>
<tr>
<td>$h$</td>
<td>Planck’s constant</td>
</tr>
<tr>
<td>$I_e$</td>
<td>Source-drain current through the electrons</td>
</tr>
<tr>
<td>$I_{eh}$</td>
<td>Current flowing from the electrons to the holes</td>
</tr>
<tr>
<td>$I_h$</td>
<td>Source-drain current through the holes</td>
</tr>
<tr>
<td>$I_{he}$</td>
<td>Current flowing from the holes to the electrons</td>
</tr>
<tr>
<td>$J$</td>
<td>Current density</td>
</tr>
<tr>
<td>$k$</td>
<td>Electron or hole wavevector</td>
</tr>
<tr>
<td>$m_0$</td>
<td>The 'bare' electron mass</td>
</tr>
<tr>
<td>$m_e^*$</td>
<td>Electron effective mass</td>
</tr>
<tr>
<td>$m_h^*$</td>
<td>Hole effective mass</td>
</tr>
<tr>
<td>$\delta n$</td>
<td>Potential asymmetry of the quantum well</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal oxide semiconductor field effect transistor</td>
</tr>
<tr>
<td>$n_{\text{B}}$</td>
<td>Density contribution from the back gate</td>
</tr>
<tr>
<td>$n_e$</td>
<td>Electron density</td>
</tr>
<tr>
<td>$n_{\text{F}}$</td>
<td>Density contribution from the front gate</td>
</tr>
<tr>
<td>$n_h$</td>
<td>Hole density</td>
</tr>
<tr>
<td>$n_s$</td>
<td>Sheet density of the 2DCG</td>
</tr>
<tr>
<td>P</td>
<td>The charge carrier momentum</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon-on-insulator</td>
</tr>
<tr>
<td>$V_{\text{B}}$</td>
<td>Voltage applied to the back gate</td>
</tr>
<tr>
<td>$V_{\text{B}}^{\text{Th}}$</td>
<td>Back gate threshold voltage</td>
</tr>
<tr>
<td>$V_e$</td>
<td>Source-drain voltage applied to the electrons</td>
</tr>
<tr>
<td>$V_{\text{F}}$</td>
<td>Voltage applied to the front gate</td>
</tr>
<tr>
<td>$V_{\text{F}}^{\text{Th}}$</td>
<td>Front gate threshold voltage</td>
</tr>
<tr>
<td>$V_h$</td>
<td>Source-drain voltage applied to the holes</td>
</tr>
</tbody>
</table>
Abstract

Semiconductors have revolutionised the field of electronics due to the nature of their readily engineerable bandstructure. Additionally, the study of the 2D charge systems hosted by devices made from these materials has led to the discovery of fundamental physics of these systems. Silicon has been at the forefront of developments in this field owing to its natural abundance, ease of processing and naturally occurring oxide. In this thesis a double gated, metal oxide semiconductor field effect transistor (MOSFET) is used to investigate a number of transport properties of electrons and holes. These include the transport properties of a single layer within a bilayer system, the control of the hole $g^*m^*$ with the MOSFET gates and probing of the effects of giant valley splitting on the electrons.

Bilayer systems are composed of two single, physically separate, layers of charge carriers contained within the same quantum well. Their study has provided insight into carrier interactions between the layers with the potential for use in vertically coupled systems of charges in novel electronic devices. Here the effects of one layer on the I-V characteristics of the other are described.

Direct control of the electron or hole spin via the gates of a transistor was first proposed by Datta and Das. Although such a device has yet to be fully realised, control of the $g^*m^*$ has been demonstrated in a number of materials. Here the control of the hole $g^*m^*$ is demonstrated on the (001) silicon plane for the first time.

Giant valley splitting is an effect whereby the valley degeneracy of the electrons in silicon is lifted. In this thesis, the effects of giant valley splitting is shown to have a similar phenomenological effect on the resistivity of a 2D electron gas as spin splitting does on the same, valley degenerate system.
Chapter 1

Introduction to the Thesis

1.1 Introduction

In this thesis silicon transistors were used to investigate a number of different transport related phenomena. To begin with, the background of semiconducting materials is introduced in a broad sense. Specific technologies and research areas are described before the items of interest in this thesis are detailed.

Semiconducting materials find uses in a wide variety of applications owing to their engineerable bandstructure. Technological applications that utilise semiconducting materials include integrated circuits and microchips, electromechanical systems, sensors and photovoltaic cells [1–7]. The continued development of these systems was spurred on by the observation of G. Moore in 1965 [8] that the number of components, specifically the transistor, that could be produced on an integrated circuit would double every 18 months. Moore’s conjecture was used by the semiconductor industry to set research and development targets for the following 50 years [9]. However, this trend in miniaturisation was predicted to end within the decade beginning in 2010 [6]. A number of solutions to this problem have been proposed and investigated; including increasing the number of gates present on the transistor as not only does this extend Moore’s Law, it also affords better control over the electronic and optical properties of the semiconductor [6]. For instance, transistors with a single gate may create and control a single layer of charge carriers within the device itself. The addition of another gate allows for the creation of two, spatially separated, layers of charge carriers; also known as a bilayer system [10, 11]. An example of a cross-section of a double-gated transistor, as used in this thesis, is shown in figure 1-1(a) while the bilayer system appears in figure 1-1(b). The vertically coupled layers within the device could add a third dimension of functionality to the currently planar integrated circuits and so provide another means by which Moore’s Law could be extended. These bilayer systems have also been used to probe carrier-carrier interactions between the two layers [10, 11].

Additional means of extending Moore’s Law can be achieved by controlling the degrees of freedom available to the charge carriers [12–15]. The field of spintronics aims to manipulate the
carrier spin in order to create devices that utilise this property to store information alongside more traditional means that manipulate charge [16]. Although a transistor capable of modulating the carrier spin in the manner described by Datta and Das [17] has yet to be created, steps have been taken towards realising this goal. One such step involves the control of the effective Landé g-factor of the carriers via the host transistor’s gates. This control has been demonstrated in a number of material systems [18–21]. For the first time, in this thesis, the effective Landé g-factor of holes is manipulated using a silicon transistor like that in figure 1-1(a).

Another degree of freedom that has been manipulated to extend Moore’s Law is the valley degeneracy present in a number of semiconducting materials [22–26]; this emerging field has been dubbed ‘valleytronics’ by a number of authors [26–28]. Valley splitting was first observed in Si/SiGe systems where the biaxial strain at the Si/SiGe interface lifted the valley degeneracy [7]. Lifting the valley degeneracy results in the lowest state in the conduction band being split into two energy levels with a measurable effect on the resistivity of the electrons in the device [23, 29]. In Si/SiGe systems this strain has been shown to increase the electron mobility and has found uses in technological applications such as the 90 nm generation of transistors [30, 31]. For the first time in this thesis the valley splitting in Si/SiO$_2$ based MOSFETs is shown to have phenomenologically similar effects on the electron resistivity as applying an in-plane magnetic field to the same, valley degenerate, system. This work has also been published in [32].

Investigations into the spin and valley degrees of freedom have received increasing attention in recent years [12–15, 18–21, 23, 25, 29, 32–40] not only due to the possibility of these being used to extend Moore’s Law, but also due to their applicability in the operation of a quantum computer [41, 42]. Silicon has been prominent in research into this subject as the advanced state of silicon electronics provides a solid foundation for building a quantum computer while the long spin-decoherence time enjoyed by the electrons in silicon means that any ‘quantum information’ stored in the coherent state may be maintained for periods as long as seconds [43, 44]. Manipulating the electron spin could conceivably be achieved in silicon by controlling the hole spin in an electron-hole bilayer system. Although this has not yet been demonstrated experimentally, Kumar et al. propose it on a theoretical basis [45]. The fact that silicon based devices are used in a wide variety of applications has potential consequences for any research into these systems [6, 46].

The introduction continues by describing the devices used for research and the major topics studied in this work.

The metal oxide semiconductor field effect transistors (MOSFETs) used for experiments in this study were silicon/silicon dioxide based devices (figure 1-1(a)). Voltages applied to the gates create inversion or accumulation regions within the central silicon quantum well. It is within this quantum well that a two-dimensional electron or hole gas, 2DEG or 2DHG respectively, were formed. With the correct application of voltages to the gates, both electrons and holes can be simultaneously present in the silicon layer. This so-called bilayer system is shown schematically in figure 1-1(b).
Silicon/silicon dioxide MOSFETs hosting a 2DEG or 2DHG are used to probe a number of previously understudied or little understood phenomena in this work. The areas of interest are summarised below.

1.1.1 The Transport Properties of a Single Charge Carrier Layer in a Bilayer System

Single 2D layers of charge carriers have been studied in a multitude of material systems under a wide range of experimental conditions for many years [47–53]. The comparatively more recent investigations into bilayer systems of charge carriers allowed inter-layer interactions to be probed and created the possibility of vertically coupled carrier layers finding uses in industrial applications [10, 11, 54]. Despite this interest in bilayer systems, few, if any, investigations into the effects of one layer on the other’s conductance properties in a bilayer system have been attempted. The only two that have were very limited in their scope as they were not actually intent on measuring this quality. The reports by Takashina et al. [29] and Morath et al. [55] focused on constant voltages and low temperatures applied to the system. In Chapter 5 it is shown for the first time that the presence of one carrier type on the conductance of the other in a bilayer system has a drastic effect on the current carrying layer.

1.1.2 Control of the Hole Effective Landé $g$-factor with the MOSFET Gates

The in-plane magnetoresistance of a 2DHG has been studied in a wide range of material systems on a number of crystallographic orientations as information about the bandstructure can be determined via these measurements [48, 56, 57]. Additionally, the control of the effective $g$-factor $g^*$ has been demonstrated in a variety of semiconducting materials with the potential to create transistors that utilise the spin degree of freedom [13, 18–21, 34, 38]. Despite its heavy use in both industry and research environments very little work in this vein has been performed on the Si (001) plane. In Chapter 6 the $g^*m^*$ of holes on the Si (001) plane is controlled via the MOSFET gates for the first time.
1.1.3 Valley Splitting

Valley splitting is an effect whereby the degeneracy of the lowest state of the conduction band is lifted [48]. This splitting is especially large at the buried oxide/silicon interface of the MOSFETs used in this study [29]. Affecting the bandstructure in this way results in a measurable change in the conduction properties of the 2DEG within the system. Three chapters investigate the valley splitting phenomena, these are detailed below.

Phenomenological Similarities between Spin and Valley Polarisation of a 2DEG

Valley splitting has been found to manifest in a number of material systems with a narrow range of absolute values that are typically smaller than other energy scales within the semiconducting system [23, 27, 48, 58–60]. In 2006 Takashina et al. [29] reported a ‘giant’ valley splitting within Si/SiO$_2$ MOSFETs. Here it is reported that the giant valley splitting has an analogous effect on the conduction properties of a 2DEG as compared to the spin polarisation of a 2DEG. This suggests some similarity in the physics underpinning both effects. Chapter 8 details the results of these experiments which were also published in [32].

Disappearance of the Giant Valley Splitting

Investigations into the giant valley splitting led to experiments attempting to discern whether the effect itself was dependent on the area occupied by the electrons at the back oxide/silicon interface of the silicon MOSFETs. However, the experiments documented in Chapter 9, demonstrate that the back oxide of the MOSFETs used were altered in such a way that the giant valley splitting was no longer present.

MOSFET Fabrication at The University of Bath

An effort was made by the author to create MOSFETs at the University of Bath using silicon wafers with a cross-sectional structure similar to that in figure 1-1(a). These devices would have allowed for further probing of the giant valley splitting. Ultimately this effort failed to produce any viable samples. For this reason, this does not appear as a chapter but instead is detailed in Appendix A.

1.2 The Rest of The Thesis

The thesis continues in Chapter 2 by considering the basic properties of the semiconductor and considering the underlying physics of the experiments. Fabrication processes used to create MOSFETs in industry are explained in Chapter 3 as many of these are important for later chapters. Chapter 4 is the last of the introductory chapters and details the experimental setups and apparatus used to obtain data. The Appendices B and C respectively contain the process sheet used to fabricate MOSFETs in Appendix A and the LabVIEW computer program used to perform measurements.
Chapter 2

Underlying Physics

2.1 Introduction

This chapter lays the foundations for the experimental chapters and begins by discussing the general properties of a bulk semiconductor with an emphasis on silicon. The effects of confinement to two dimensions on the bandstructure of silicon are shown and charge transport through such a system is analysed using the Drude model. Both the Hall and quantum Hall effects are introduced here as they are used as an analytical tool in later chapters. Additionally the practical operation of a Si-MOSFET and an explanation of the valley splitting effect are detailed.

2.2 The Bandstructure of Silicon

The physical structure of a material, be it an insulator, metal or semiconductor, underpins a number of important quantities including the bandstructure of the substance. Like other Group IV elements, silicon possesses the diamond structure, an example of which is shown in figure 2-1. As described in Chapter 1 the bandstructure is responsible for the electronic and optical properties of a substance. A schematic diagram of the bandstructure of silicon, showing the conduction band minima and valence band maxima, is depicted in figure 2-2. Models of the bandstructure are typically based \([61–68]\) on the envelope function approximation (EFA) and \(\mathbf{k} \cdot \mathbf{p}\) method \([69]\). These are described below.
Figure 2-1: From [70]. The diamond structure exhibited by Group IV elements. Where silicon is concerned the unit cell length $a = 0.543$ nm.

### 2.2.1 $\mathbf{k} \cdot \mathbf{p}$ Model and EFA

Initially the major results of the $\mathbf{k} \cdot \mathbf{p}$ model and EFA are described here followed by an explanation of the importance of the spin-orbit interaction in both the wider literature and this report.

The most basic model of the bandstructure of an indirect bandgap semiconductor results in the energies $E_C(k)$ for the conduction band and $E_V(k)$ for the valence band [70]

$$
E_C(k) = \frac{E_G}{2} + \frac{\hbar^2 (k - k_0)^2}{2m_C^*}, \quad E_V(k) = \frac{E_G}{2} - \frac{\hbar^2 k^2}{2m_V^*}
$$

(2.1)

where $k$ is the wave vector, $k_0$ the point at which the conduction band minimum occurs in $k$-space, $E_G$ the band gap and $m_C^*$ and $m_V^*$ are the effective masses for the conduction and valence bands respectively [70, 71]. A more realistic model must account for nonparabolicity, anisotropy and the coupling between heavy and light holes. To account for these details of the bandstructure both the EFA and $\mathbf{k} \cdot \mathbf{p}$ method are used in combination with quasi-degenerate perturbation theory to generate Hamiltonians that describe $E_C(k)$ and $E_V(k)$ It is by using these methods that the bandstructure in figure 2-2 is generated [69, 71]. The Hamiltonian $\hat{H}$ that describes the periodic potential of the lattice and spin orbit interaction is

$$
\hat{H} = \hat{H}_0 + \hat{H}_{SO}
$$

(2.2)

$$
E_\nu(k) \Psi(k) = \left( -\frac{\hbar^2}{2m^*} \nabla^2 + V_0 - \frac{\hbar}{4(m^* c)^2} \mathbf{p} \cdot \sigma \times (\nabla V_0) \right) \Psi(k)
$$

(2.3)

where $\hat{H}_0$ is the Hamiltonian describing the periodic potential of the lattice and $\hat{H}_{SO}$ contains the details of the spin orbit interaction. Specifically, $\nu$ is the band index, $\Psi$ the carrier wavefunction, $\hbar$ is Planck’s constant, $m^*$ the effective mass, $\mathbf{p}$ the momentum $V_0$ is the microscopic lattice-periodic potential and $\sigma$ is the vector of Pauli spin matrices [71]. One of the major advantages of the EFA and $\mathbf{k} \cdot \mathbf{p}$ methods is that they can handle the application of externally applied magnetic and electric fields to the system being modeled. Under an applied magnetic
field the momentum operator undergoes the transformation $p \rightarrow p - eA$ where $A$ is the magnetic vector potential. Accounting for these fields produces the effective mass Hamiltonian

$$\hat{H} = \left( -\frac{i\hbar \nabla - eA}{2m^*_n}\right)^2 + V(r) + \frac{g^*_n}{2} \mu_B \sigma \cdot B$$

(2.4)

where $A$ is the magnetic vector potential and $\mu_B$ is the Bohr magneton. The carriers in the $n$th energy band were treated as though they were free particles with an effective mass $m^*_n$ and an effective Landé $g$ factor $g^*_n$ under the influence of an externally applied potential $V(r)$ [69, 71]. In real experiments these parameters along with the bandgap are chosen such that they give good agreement with data from optical spectra and cyclotron resonance [72].

Figure 2-2: From [71]. The bandstructure of silicon in the [001] direction. $k_0$ demarcates the location of the minimum in the conduction band.

The spin orbit interaction arises from the motion of a charged particle through an electric field that is at rest with respect to the moving charge carrier. This stationary electric field has a few origins; the most immediate for an electron in a material is the potential generated by the nucleus of the atoms in the substance. Another, the Dresselhaus effect, stems from certain materials that possess a physical structure that lacks inversion symmetry [73]. Silicon contains
a physical structure that has inversion symmetry and so does not induce the Dresselhaus effect on charge carriers - although the 'bare' effect of the silicon nucleus on the electron is still present [71]. Instead, when applying an external electric field to a host of electrons or holes via the gates of a MOSFET, the Rashba effect must be accounted for. This effect is dependent on the momentum of the carriers and results in the angular momentum $j$ of the hole states at the top of the valence band taking values $j = 3/2$ [71]. This value changes with confinement to a 2D state, as will be discussed later. An understanding of the spin-orbit interaction has resulted in a deeper insight into fundamental quantities of 2D carrier systems. A report by Pudalov et al. generated the controversial findings that the metallic state of a 2D charge carrier system could be inhibited by a magnetic field applied in the plane of the 2D carriers [74]. In that report they suggest their results could be a consequence of the SO coupling. Further investigation of this effect was proposed by use of samples with a tunable spin splitting. As described in Chapter 1, Datta and Das proposed a type of transistor in which the current was modulated via SO coupling while magnetised contacts selectively inject and detect specific spin orientations [17]. Research into the creation of such a device has been underway for a number of years [75] and was demonstrated in a number of material systems [18, 76–78]. However, no-one has yet demonstrated this on the Si (001) plane of a Si-MOSFET. In Chapter 6 of this thesis the control of the $g^*$-factor on the [001] plane of an Si-MOSFET is demonstrated using the gates of the device.

### 2.2.2 The Exchange Interaction

When investigating the effective $g$-factor it is important to consider the exchange interaction as the $g$-factor is essentially determined by the difference of the exchange interactions of up- and down-spin electrons in the vicinity of the Fermi level [48]. This interaction can lead to overestimates of $g^*$ in theoretical calculations that utilise the single particle model because the effect reduces the energy difference between the polarised and unpolarised states [71, 79, 80]. The exchange interaction can be described by the following equation [71]

$$\hat{H}_{\text{ex}} = -\sum_{m} J(r - R_m) S_m \cdot \sigma$$  \hspace{1cm} (2.5)

where $\sigma$ is the spin operator of the electrons in the conduction and valence bands, $S_m$ is the operator for the total spin of an electronic shell at position $R_m$. The function $J(r - R_m)$ describes the exchange interaction while the sum runs over all atoms in the host material [71, 80]. Including equation 2.5 in the $k \cdot p$ model is achieved by adding $\hat{H}_{\text{ex}}$ to equation 2.2.

The above has ramifications for later chapters where the magnetic field required to fully spin polarise a given density of electrons or holes is used to determine the effective $g$-factor.

### 2.2.3 The Bulk Structure of the Conduction and Valence Bands

Calculating the dispersion relation of silicon in the [001] direction using the $k \cdot p$ results in a broad variety of features that have been described in depth elsewhere [70, 71]. In this section
the results in bulk silicon that are pertinent to the research in this thesis are considered. These are the minimum in the conduction band away from the Γ point and the heavy-hole light-hole coupling in the valence band in the vicinity of the Γ point (figure 2-2).

When electrons occupy states in the conduction band they do so in the minimum at \( k = 0.84\pi/a \) in the \( \Delta \) direction (figure 2-2). The immediate vicinity either side of \( k = k_0 \) can be modeled by assuming a simple quadratic dispersion relation of the form given in equation 2.1. Plotting these regions as surfaces of constant energy as a function of \((k_x, k_y, k_z)\) produces the figure in 2-3. These surfaces are 6-fold degenerate and become important when confinement to a quantum well is considered later.

![Figure 2-3: The 6-fold degenerate surfaces of constant energy in bulk silicon.](image)

At the Γ point the valence band is degenerate and the heavy and light holes are indistinguishable. Away from the Γ point the degeneracy lifts and, due to the SO interaction, the light holes gain an angular momentum of \( j = 1/2 \) while the heavy holes gain \( j = 3/2 \). As described in the previous section, the coupling between the light and heavy holes must be accounted for in order to obtain a more accurate understanding of the valence band structure. The coupling is expressed within the off-diagonal components of the \( \mathbf{k} \cdot \mathbf{p} \) Hamiltonian and become larger with increasing \( k \) [71]. The coupling between the light and heavy holes is of interest when the system is confined as will be explained later.

### 2.3 The Effects of Confinement

In this section the effects of confining electrons or holes to the [001] plane, as is the case in the MOSFETs used in this report, are discussed. Confinement affects both the conduction and valence band with different results for both electrons and holes. Both of these are considered separately below.
2.3.1 The Conduction Band and Valley Splitting

Confining the electrons to two dimensions at the Si/SiO$_2$ interface, as is done in the SOI layer of the MOSFETs in this study, means that the two $k_z$ states in figure 2-4 become degenerate in energy with respect to each other. The remaining four-fold degenerate states, also shown in figure 2-4, are at a greater energy than the two-fold degenerate $k_z$ states. This difference in energy means that the $k_z$ states are occupied first as the Fermi level passes through them. This is followed by the occupation of the $k_x$ and $k_y$ states; this process is shown schematically in figures 2-4(b)(i) and 2-4(b)(ii).

![Diagram of valley splitting](image)

Figure 2-4: The 4-fold and 2-fold degenerate states on the Si (001) surface. The 2-fold degenerate states lie above and below the plane of the paper, along the z-axis. (b)(i) Shape of the Fermi surface when only the lower $k_z$ state is occupied. (ii) Electrons start to occupy the $k_x$ and $k_y$ states, creating the Fermi surface shown here.

The $k_z$ states possess a heavier effective mass than the $k_x$ and $k_y$ states and, due to confinement within the quantum well, are separated in energy as depicted schematically in 2-5(b). The degeneracy of the lower, 2-fold degenerate states in figure 2-5(b) can be lifted using either strain at the oxide/semiconductor interface [7] or by application of a gate voltage [29]. It should be stressed that when this degeneracy is lifted the effective masses of the electrons occupying each level are identical. This process is known as valley splitting and is shown schematically in figure 2-5(b)(i-iii). Experimentally, valley splitting was measured as a change in the conductance characteristics of a 2DEG with typical values of the valley splitting at certain SiO$_2$/silicon interfaces found to be no larger than 0.1 and 2 meV [48, 81–85]. Other materials such as SiGe [36, 86], AlAs [23] and, more recently MoS$_2$ [26, 27], have also demonstrated valley splittings. The valley splittings observed in strained systems and Si/SiO$_2$ MOSFETs have different origins. In strained systems, it is the strain itself that lifts the degeneracy between pairs of valley states [7, 30, 59]. In Si/SiO$_2$ MOSFETs the degeneracy of the $k_z$ pair itself is lifted [87, 88]. By considering perturbation theory and the abruptness of the Si/SiO$_2$ interface, it is possible to demonstrate that there is a greater coupling between the two $k_z$ states for perfectly abrupt interface. That is, the potential barrier between the silicon and silicon dioxide is a step function. This leads to a greater valley splitting in these material systems [87]. It is these differences
between Si/SiO$_2$ systems and strained materials that give rise to different effects on the electron mobility. In Si/SiGe, the valley splitting induced by strain raises the electron mobility whilst in the electron mobility is reduced [7, 29].

![Diagram](image)

Figure 2-5: (a) From (i) to (ii): Confining the 6-fold degenerate system to a 2D plane lifts the degeneracy and gives rise to energy levels dependent upon the effective mass of the electron. Moving from (i) to (ii) is akin to moving from figure 2-3 to figure 2-4. (b) From (i) to (iii): An out of plane electric field is used to lift the the valley degeneracy $\Delta_V$ of the 2-fold degenerate state. Under sufficiently large fields the electrons populate only the lower (+) valley at which point the system is said to be valley polarised.

It was reported in 2006 by Takashina et al. that there existed a giant valley splitting at the SIMOX oxide/silicon interface present in many double-gated MOSFETs [29]. This 'giant' valley splitting was found to exceed 30 meV under large gate biases. Although theoretical considerations of the valley splitting have shown that its magnitude is affected by features at the oxide/silicon interface [89, 90], it was only recently in 2010 that a theory proposed by Koiller et al. [87] could correctly predict the size of the splitting observed by Takashina et al. It is the giant valley splitting that forms the basis of experimental chapters 8 and 9.

2.3.2 The Valence Band

Under confinement to two dimensions the 4-fold degeneracy of the $j = 3/2$ states at the top of valence band where $k = 0$ in figure 2-1(b) lift producing the system in 2-6. The $z$ component of the angular momentum $m$ for heavy (HH) and light holes (LH) becomes $m = \pm 3/2$ and $m = \pm 1/2$ respectively. Under these confined conditions, the nature of the SO coupling with the holes in the valence band changes [71]. Additionally, with sufficient confinement, there will be minimal mixing of the LH and HH states which was predicted to result in a highly anisotropic effective $g$-factor for the heavy holes [33]. Experimentally it was shown that, by applying an electric field with the gates of a transistor to a 2DHG, $g^*$ could be controlled [18, 76–78]. These experiments were conducted in GaAs and InAs based systems and the results were attributed to the Rashba mechanism as this splits the spin of the holes. Although control of $g^*$ has been
demonstrated in silicon quantum nanowires [91] and SiGe quantum dots hosting holes [92] no similar work has been performed on the Si (001) plane. In this thesis, for the first time, control of the effective $g$-factor is demonstrated on the Si (001) plane. The results are presented in Chapter 6.

Figure 2-6: (a) Confinement lifts the degeneracy of the heavy and light hole bands shown in figure 2-1(b). (b) Taking the effects of confinement, SO interaction and heavy-hole light-hole coupling into account.

2.4 Generating a 2DEG or 2DHG within the Silicon Quantum Well

In this section the structure of the Si/SiO$_2$ MOSFETs is discussed and the practical methods used to generate a 2DEG or 2DHG within the central silicon layer described. The MOSFET itself is composed of a number of different layers as shown in the schematic cross-section in figure 2-7(a). Starting at the bottom of the device, the silicon substrate is slightly p-type and acts as the back gate for the device. Above this the buried oxide (BOX) is the gate oxide for the back gate. The monocrystalline silicon-on-insulator (SOI) layer is selectively doped with n- or p-type dopants to create contacts to any carriers present within the layer. The front oxide above the SOI layer acts as the gate oxide for the polycrystalline silicon front gate. Finally, metal contacts connect the n- and p-type regions of the SOI layer to the rest of the circuit. Figure 2-7(b) shows a plan view of this with the different contact types labeled and the SOI layer visible through both the poly-silicon and the front oxide.
Generating a 2DEG or 2DHG within the SOI layer requires the application of a voltage to one of the gates. Consider the situation where both front and back gate voltages, $V_F$ and $V_B$ respectively, are set such that the conduction and valence bands are flat within the quantum well. Under these conditions the quantum well is symmetric and, initially, it will be assumed there are no charge carriers in the well (figure 2-8(a)). Assuming $V_B = 0$ V while applying a positive front gate voltage will cause a positive charge to accumulate at the poly-Si/FOX interface. In response to this the conduction and valence bands in the SOI layer close to the FOX/SOI interface bend to accommodate for this excess charge. Under a sufficiently positive $V_F$ the bottom of the conduction band intersects with the Fermi level and a 2DEG is formed in the newly formed inversion layer (figure 2-8(b)) [51, 70]. Additionally, a 2DHG can be generated at the FOX/SOI interface by again applying $V_B = 0$ V while also applying a negative front gate voltage. Here an accumulation region containing a 2DHG is formed in the valence band when the Fermi level intersects with the top of the valence band [51, 70] (figure 2-8(c)). For large gate voltages of opposite sign the conduction and valence bands are sufficiently warped to allow for both a 2DEG and a 2DHG to simultaneously exist within the SOI layer (figure 2-8(d)). Figures 2-8(a) to (d) can be reflected in the y-axis in the case where positive or negative voltages are applied to the back gate.
Conduction band
Valence band
Back
Front
h
E
z

Figure 2-8: (a) The bands are flat when both gate voltages are zero. (b) A positive voltage is applied to the front gate generating a 2DEG at the front interface. (c) A negative voltage is applied to the front gate generating a 2DHG at the front interface. (d) Large voltages of opposite sign are applied to the gates creating an electron-hole bilayer.

2.4.1 Calculating the Potential and Carrier Wavefunction within the Quantum Well

In applying gate voltages the electric field in the well changes accordingly. Once a certain threshold voltage has been exceeded a 2DEG or 2DHG will form at one of the interfaces. It is quite possible to generate two layers of electrons, holes or even an electron-hole bilayer under the correct conditions. Determining where in the well the carriers exist is important because that provides information as to how close the carriers are to a given interface. The closer the carriers to the interface the greater the interaction with the disorder potential at that interface. In order to determine both the wavefunction and shape of the quantum well both the Schrödinger and Poisson equation for the electric field must be self-consistently solved.

\[
\left( \frac{(-i\hbar)^2}{2m^*} \frac{\partial^2}{\partial z^2} + V(z) \right) \Psi = E(z) \Psi \tag{2.6}
\]

\[
-\frac{\partial^2 V(z)}{\partial z^2} = \frac{\rho_c}{\epsilon} \tag{2.7}
\]

where \(V(z)\) is the potential profile inside the quantum well, \(\rho_c\) is the charge density induced by the gates and \(\epsilon\) is the electrical permittivity of the medium hosting the charge carriers. Typically the wavefunction \(\Psi\) will be needed for a given electric field within the well. A usual starting place are gate voltages that produce a flat band within the well as this has a well known solution [70]. Once these gate voltages have been found using equation 2.7 the potential in the well is changed by a small amount based on the final desired gate voltages. This new potential
is substituted back into the Schrödinger equation in order to determine the new wavefunction. This process is repeated until the final gate voltages are reached.

![Diagram of quantum well deformation](image)

**Figure 2-9:** From (a) to (c) the quantum well is progressively deformed by the application of ever increasing gate voltages. The electronic wavefunction (blue line) moves according to the solution of the Schrödinger and Poisson equations.

Having described how to generate a layer of charge carriers in the MOSFET, the transport properties of such a system will be described. These properties are modeled using the Drude model which is described below. Additionally the quantum and normal Hall effects are discussed as they were used to determine carrier densities in experiments.
2.5 The Drude Model and the Hall Effect

When applying an electric and/or magnetic field to a material the electrons or holes within that material will experience a force. Treating the carriers as though they had an effective mass \(m^*\), a time between scattering events \(\tau\) and considering the total force on the particles due to the externally applied fields results in the Drude Model [70]:

\[
m^* \left( \frac{d\mathbf{v}}{dt} + \frac{\mathbf{v}}{\tau} \right) = q(\mathbf{E} + (\mathbf{v} \times \mathbf{B}))
\]  

(2.8)

where \(\mathbf{v}\) is the velocity of the carriers, \(q\) is the electronic charge and \(\mathbf{E}\) and \(\mathbf{B}\) are respectively the electric and magnetic fields. For a given carrier type of mass \(m^*\) the current density \(\mathbf{J}\) can be related to the electric field via the relationship

\[
\mathbf{E} = \rho \mathbf{J}
\]

(2.9)

where \(\rho\) is the resistivity tensor. For a 2D carrier gas (2DCG) in the x-y plane with a magnetic field applied in the z-direction, as in figure 2-10. \(\rho\) is given by the 2x2 matrix

\[
\rho = \begin{bmatrix} \rho_{xx} & \rho_{xy} \\ \rho_{yx} & \rho_{yy} \end{bmatrix}
\]

Onsager\[\rightarrow\]

\[
\rho = \begin{bmatrix} \rho_{xx} & \rho_{xy} \\ -\rho_{xy} & \rho_{xx} \end{bmatrix}
\]

(2.10)

where it has been assumed that there is no current flowing in the z-direction \((J_z = 0)\) and the electric fields in the y and z directions are equal to zero. Assuming Onsager reciprocity the, argument on the left side of equation 2.10 undergoes the transformation shown by the arrow [93]. Experimentally the transverse and longitudinal voltages, \(V_{xy}\) and \(V_{xx}\) respectively, are measured as shown in figure 2-10.

![Figure 2-10: (a) Measurement setup for the Hall effect with a sample of width \(W\) and length \(L\). The Hall voltage \(V_{xy}\) can be measured between probes 3 and 5 or 4 and 6. (b) Plan view of (a) with the voltage probes removed and the current path of the charge carriers under the influence of the magnetic field.](image)

27
These quantities allow the carrier density and mobility to be calculated via the relations

\[
\rho_{xx} = \frac{WV_{xx}}{LT} = \frac{1}{n_s e \mu}, \quad \rho_{xy} = \frac{WV_{xy}}{LT} = \frac{B}{n_s e}
\]  

(2.11)

This, however, is not the entire picture as any misalignment between the voltage probes must be taken into account as these would lead to errors when measuring \(V_{xy}\). Using equations 2.8, 2.9 and 2.10 it can be shown that when the magnetic field is reversed \(\rho_{xx}\) and \(\rho_{xy}\) are respectively even and odd functions

\[
\rho_{xx}(+B) = \rho_{xx}(-B) \\
\rho_{xy}(+B) = -\rho_{xy}(-B)
\]  

(2.12) (2.13)

thus

\[
\rho_{xx}(+B) = \frac{W}{2L}(R_{xx}(+B) + R_{xx}(-B)) \\
\rho_{xy}(+B) = \frac{1}{2}(R_{xy}(+B) - R_{xy}(-B))
\]  

(2.14) (2.15)

Although this method can account to a certain degree for the inclusion of \(R_{xx}\) in the measured \(R_{xy}\) signal, it cannot fully remove its presence under certain conditions. These conditions are present at low carrier densities where \(\rho_{xx}\) will be large and magnetic fields where \(\rho_{xy}\) becomes similar in magnitude to \(\rho_{xx}\). This introduces a high degree of noise in the measured \(R_{xy}\) signal making it more difficult to extract an accurate value of the carrier density using this method [70]. An experimental example of this is shown in Chapter 5.

Equations 2.11 agree well with Hall’s original measurements in 1879 [94]. However, later they were found to need modifying at lower temperatures where the quantum Hall effect appears. It is also possible to determine carrier densities via the quantum Hall effect without the need to resort to equations 2.12 through 2.15.

2.5.1 The Spin Polarisation of a 2DCG

So far in the discussion of the application of a magnetic field to a 2DCG nothing has been stated about the carrier spins and the effect of this field on those spins. This is considered in this section. Under a sufficiently large magnetic field the carriers in the 2D system will align themselves with the magnetic field such that their spins are either parallel or anti-parallel to the field. The following is assumed about the 2D charge carrier system under scrutiny in this section. The 2DCG is initially spin degenerate on the Si (001) plane in an Si-MOSFET with a sheet density \(n_S\) and 2D density of states \(D_0 = \frac{m^* m_0}{\pi \hbar^2}\) for each spin subband and where \(m_0\) is the free electron mass (figure 2-11(a)) [70]. Additionally, there is no broadening of the subband energy levels. As in the experiments described later in this thesis, applying an in-plane
magnetic field this 2D system lifts the spin degeneracy and introduces a Zeeman splitting $\Delta_Z$ of the upper ($\uparrow$) and lower ($\downarrow$) spin subbands (figure 2-11(b)). Under sufficient magnetic field the upper spin subband in depopulated (figure 2-11(c)) and the carrier density occupying the lower subband density can be written as $n = D_0 \Delta_Z$.

![Diagram of spin degenerate, split, and polarised states](image)

**Figure 2-11:** (a) to (c) show schematically the progressive spin polarisation of the spin subbands of the 2DCG with magnetic field. $E_F$ is the Fermi level.

Here it will be assumed that the carriers are some generic particle with a certain spin and effective mass. In later chapters the masses and $g$-factors of the electrons and holes will be substituted into the following equations where relevant. The Zeeman splitting can be written as

$$\Delta_Z = g^* \mu_B B$$  \hspace{1cm} (2.16)

where $B$ is the magnetic field, $g^*$ the effective Landé $g$-factor, $\mu_B$ is the Bohr magneton given by $e\hbar/2m_0$. Equation 2.16 can be rewritten as

$$\Delta_Z = g^* \mu_B B$$  \hspace{1cm} (2.17)

At full spin polarisation $B = B_P$ and $\Delta_Z = n_S/D_0$. Substituting $B_P$ into equation 2.16 and equating it with $n_S/D_0$ gives

$$n_s \frac{2\pi \hbar^2}{m^* m_0} = g^* \mu_B B_P$$  \hspace{1cm} (2.18)

Additionally, substituting for $\mu_B$ results in the expression

$$g^* m^* = 2 \frac{n_s \hbar}{B_P c}$$  \hspace{1cm} (2.19)

Equation 2.19 will be used later when determining the effective $g$-factor of both the electrons and holes.
2.6 The Integer Quantum Hall Effect (QHE) and Shubnikov de-Haas Oscillations

This effect was apprehensively [48] predicted by Ando et al. in 1975 [95] and was unexpectedly discovered and reported by von Klitzing in 1980 [96]. The main results of that study are repeated in figure 2-12.

![Diagram of Hall probe setup with voltage plots](image)

**Figure 2-12: From [96].** The Hall voltage $U_H$ and the voltage drop $U_{PP}$ between the probes (where $U_{PP}$ is equivalent to $V_{xx}$ in figure 2-10) are both plotted as a function of the gate voltage $V_g$. Troughs and plateaus, signatures of the QHE, can be clearly seen in $U_{PP}$ and $U_H$ respectively.

The plateaus in $V_{xy}$ and troughs in $V_{xx}$ appear for the following reasons. Consider an Si-MOSFET hosting a 2DEG of constant density. At zero magnetic field the density of states of this 2D system is a constant function of energy given by

$$g_{2D} = \frac{m^* m_0}{\pi \hbar^2}$$  \hspace{1cm} (2.20) 

where $m^*$ is the effective mass of the carriers and $m_0$ the free electron mass [70](figure 2-13(a)). Applying a magnetic field causes the electrons to act like simple harmonic oscillators with
energies $E_n$ where $n$ is an integer. The frequency with which the carriers orbit the magnetic flux lines is given by the cyclotron frequency $\omega_c = eB/m^*$ [70, 97]. The effect of this on the density of states is shown in figures 2-13(b) and 2-13(c). As the magnetic field increases the states available to the electrons group together into Landau Levels separated by the cyclotron energy with regions between the Levels where there are no allowed states [70]. Simultaneously, the Landau Levels move relative to $E_F$ as the magnetic field is increased. When the Fermi level lies in a gap, as it does in figure 2-13(c), electrons cannot move to new states and so there is no scattering. As a result of this the transport through the MOSFET is dissipationless and $V_{xx}$ goes to zero. Additionally, the plateaus in $V_{xy}$ appear as the edge currents in the Hall bar become quantised in units of $Ih/2e^2$. Note that although the above argument has assumed a fixed Fermi energy and electron density, the same effect can also appear for a fixed magnetic field and changing carrier density. The electron density would be altered by manipulating the gates of the device.

All of the carriers may occupy a single Landau level. In this instance the ratio of the total carrier density to the density within a Landau level is equal to one. This ratio is given by $\nu = n_s/(eB/h)$ where $\nu$ is the filling factor, $n_s$ is the carrier density and $(eB/h)$ is the density of carriers in the Landau level. The effects of valley and spin splitting on the Shubnikov-de Haas oscillations are discussed after considering the effects of the magnetic field on the carrier momentum.

Under the influence of the magnetic field the momentum of the carriers becomes $\mathbf{p} - e\mathbf{A}$ where $\mathbf{A}$ is the magnetic vector potential. Using the Landau gauge for the magnetic vector potential gives $A_y = Bx$, $A_x = 0$ [97]. Utilising these and considering a single particle, the Schrödinger equation can be written

$$\frac{(-i\hbar \nabla - e\mathbf{A})^2}{2m^*} \Psi = E_n \Psi$$

(2.21)
where the potential has been set zero and $\Psi$ is the wavefunction of the carriers in the $x-y$ plane. This results in the energies $E_n$

$$E_n = \left(n + \frac{1}{2}\right) \hbar \omega_c$$

(2.22)

where $\omega_c$ is the cyclotron frequency given by $eB/m^*$. Plotting $E_n$ as a function of $B$ produces a fan diagram (figure 2-14).

![Figure 2-14: (a) A fan diagram with the first four $E_n$ plots shown. (b) A fan diagram similar to that shown in (a) but the vertical axis is in sheet density instead of energy.](image)

Experiments like those performed in this thesis do not produce data like that in figure 2-14(a) as the transmission spectra of the charge carriers are not measured. Instead, the resistivities $\rho_{xx}$ and $\rho_{xy}$ are measured as a function of field at low temperatures ($T \approx 2$ K). The data produced by these measurements are identical to those presented in figure 2-12. It is from these plots of $\rho_{xx}$ and $\rho_{xy}$ that the carrier densities of the 2D carrier gas (2DCG) are extracted. The equations for the total carrier density in the quantum well and the filling factor $\nu$ can then be used to plot the diagram in figure 2-14(b). These equations are shown below

$$n_s = C_F(V_F - V_{F}^\text{Th}) + C_B(V_B - V_{B}^\text{Th}), \quad n_s = \nu \frac{eB}{\hbar}$$

(2.23)

where $C_F$ and $C_B$ are the front and back capacitances between the relevant gate and the 2DCG respectively and $V_{F}^\text{Th}$ and $V_{B}^\text{Th}$ are respectively the front and back gate threshold voltages [51, 70]. The data extracted from experimental data can be compared to the lines generated by the equations in order to check the accuracy of the extracted data with respect to theory. This is performed and presented in later chapters.
2.6.1 The Effects of Spin and Valley Splitting on Shubnikov-de Haas Oscillations

To explain how Shubnikov-de Haas Oscillations are modified by the presence of spin and and valley splitting data from work by Takashina et al. will be used [29]; the data itself is fully described in Chapter 7. Figure 2-15(a) shows a greyscale plot of the second derivative of the source-drain electron conductance through a Si/SiO\textsubscript{2} MOSFET. The data was obtained over a range of front and back gate voltages \( V_F \) and \( V_B \) respectively. In figures 2-15(b) a perpendicular magnetic field of 5.5 T has been applied to the system in order to the lift spin degeneracy. Figure 2-15(c) shows the same data as that in figure 2-15(b) but with a different contrast and a number of different features present in figure 2-15(b) identified. It should be noted that all data in figures 2-15(a) to (c) were obtained at a temperature of 4.2 K.

Feature A corresponds to when the second spatial subband has been occupied, or alternatively, when there are electrons at both the front and buried oxide/SOI interfaces. Features B and C delineate the occupation of the upper valley subband and the onset of conduction respectively. The origin of these features are explained in greater detail in Chapter 7. As both the spin and valley degrees of freedom are degenerate in figure 2-15(a), it would be expected that the change in the total filling factor of the system \( \Delta \nu^{TOT} \) would be equal to 4 [97]. Between features A and B the system is valley polarised while only for gate voltages between features B and C is the system fully valley polarised and so \( \Delta \nu^{TOT} \) should equal 2 here. The application of the magnetic field has lifted the spin degeneracy in figure 2-15(b) revealing the Shubnikov-de Haas oscillations and associated filling factors \( \nu \) of the system. The lines of constant filling factor were calculated and plotted over those in figure 2-15(b), creating the pattern in figure 2-15(c). In figure 2-15(c) \( \nu^+ \) and \( \nu^- \) are the lower and upper valley subband filling factors respectively. At small gate voltages, the system is valley degenerate (top left of figure 2-15(c)) and the periodicity of the total filling factor is \( \Delta \nu^{TOT} = 4 \) as this is the combined degeneracy of spin and valley degrees of freedom. Valley polarising the system under this magnetic field forced \( \Delta \nu^{TOT} \) to halve to 2 as the only degeneracy left was due to spin [29]. Thus the effect of valley polarisation on the Shubnikov-de Haas oscillations of a spin split system is to halve their periodicity. A similar result is expected for a valley degenerate system that is spin polarised [97].
The exchange interaction also plays an important role in the separation and relative motion of Landau levels as they are occupied. This process is depicted schematically in figure 2-16 [48, 83]. The different spin orientations are represented by $\uparrow$ and $\downarrow$ and the valley subbands $+\nu$ and $-\nu$. The occupied levels experience a self-energy shift proportional to their occupation and inversely proportional to the screening of the system. A significant energy gap between the lowest filled subband and the next, unoccupied state exists in figure 2-16(b) as a result of this [48]. The enhancement oscillates with the occupation of the Landau levels and gives rise to metallic and insulating states; metallic when $E_F$ lies in a partially occupied subband (figures 2-16(a), (c), (e) and (g)) and insulating when $E_F$ lies in a region between subbands (figures 2-16(b), (d) and (f)).
Figure 2-16: From [83]. (a) to (c): Occupied levels (shaded red) experience a self-energy shift proportional to their occupation and inversely proportional to the screening of the system. The enhancement is large in an insulating system as in (b), (d) and (f) and small in a metallic situation as in (a), (c), (e) and (g) [48].

2.7 Closing Comments

Having introduced the physics underlying the experiments it is now pertinent to move on to the second of the introductory chapters in which the major fabrication steps used to make a MOSFET are outlined and explained.
Chapter 3

Fabrication of MOSFETs

3.1 Introduction

In this chapter the industrial fabrication processes used to produce the MOSFETs studied in this thesis are described and explained. Starting with the creation of the silicon substrate, the chapter continues with the formation of the oxide layers and silicon-on-insulator layer, front gate and electronic contacts. Techniques that underpin these steps are described and explained with focus drawn to those used in the fabrication of MOSFETs used in this study. Additionally some of the processes used in Appendix A to create MOSFETs at The University of Bath are touched upon in this chapter.

3.2 MOSFET Cross-section

To give a full account of every transistor and their production processes would be extremely unwieldy here due to the large body of information on the subject [51, 98–101]. The structure in 3-1(a) is focused upon as it and the techniques used to fabricate it are quite common. The figure shows a schematic cross-section of the final MOSFET product that results from the fabrication processes described in this chapter. These layers are, from bottom to top, the silicon substrate, the buried oxide (BOX), the silicon-on-insulator (SOI) layer with doped regions labeled n/p, the polycrystalline silicon front oxide (FOX) and the aluminium contacts to the rest of the circuit. Post-fabrication, the wafer will have an array of transistors on its front surface as shown in figure3-1(b). Operation of the transistors was described in chapter 2 and so will not be repeated here.
3.2.1 MOSFET Geometry

When fabricating MOSFETs a range of different mesa geometries are available to the experimentalist. The shape of the SOI layer will depend upon the quantities to be measured and the accuracy with which these quantities are to be measured. In this section two widely used device geometries that are pertinent to this thesis are discussed.

Figures 3-2(a) and (b) show the Hall Bar geometry and Corbino disc arrangement. Hall Bars are frequently used as they allow for the determination of the Hall voltage and other quantities described in Chapter 2 to a high degree of accuracy [102]. The rectangular shape of the Bar, defined by mesa etching, is readily mass produced and so ideal for industrial applications [51, 102].

Current in the Corbino disc (figure 3-2(b)) flows radially outwards from source-drain contact 1 to contact 2. If a magnetic field is applied perpendicularly to the plane of the sample then there will be no accumulation of charge as there would be when using the Hall Bar in figure 3-2(a). As there are no edges for charge to build up on, the carriers follow a spiral route out from contact 1. This means that there is no Hall voltage in these devices [70].
Figure 3-2: For all figures the shaded, numbered areas correspond to Ohmic contacts. (a) Hall bar geometry; the current is applied between contacts 1 and 2 and the Hall voltage measured across contacts 3 and 5 or 4 and 6. (b) A Corbino disc; here the transverse resistivity and Hall voltage are eliminated.

### 3.3 Creating The Substrate

The wafers were cut from a silicon ingot that was produced via the Czochralski (CZ) process (figure 3-3). In this process, silicon is melted in a quartz furnace and doped with n- or p-type dopants such as phosphorus or boron to the required dopant density. A monocrystalline silicon ‘seed’ is inserted into the molten silicon [100, 103]. The seed is then slowly lifted and simultaneously rotated. The speed of rotation and lift away from the melt determines the diameter of the resulting ingot. Once it has cooled the silicon is cut into 200 to 750 µm thick wafers [103]. This method produces the ‘nine-nines’ (99.9999999%) purity required of the silicon for electronic grade material [103].
3.4 The Buried Oxide and Silicon-On-Insulator (SOI) Layer

SOI is, as the name implies, a layer of silicon atop an insulator; in this case that insulator is SiO₂. Thicknesses of the silicon layer range from nanometers to micrometres. Different methods are used to create a layer of this size. Two approaches are described here, the SIMOX (Separation by IMplantation of Oxygen) and another that involves the bonding and splitting of wafers. Although both methods are used to implant ions into the silicon substrate the ionic species and goals of each are different. The SIMOX process uses oxygen ions to create a layer of oxide in situ within the silicon. This was the method by which buried oxides were formed in MOSFETs used in this study. Where wafer bonding is concerned hydrogen ions are implanted into the silicon substrate enabling a thin, uniform layer of silicon to be transferred to another substrate such as silicon dioxide [101, 104]. It is these techniques that ultimately allow for the creation of the double gate structure.

Figure 3-3: (a) The silicon is heated until it melts. (b) A monocrystalline silicon seed is lowered into the melt. (c) The seed is rotated and lifted out of the melt. The surface tension of the molten silicon ensures the material is dragged upwards by the seed. (d) As the seed is lifted the silicon cools and forms a crystal. (e) The fully formed silicon ingot. Some residue is left over from the process.
3.4.1 SIMOX

The concept of forming an oxide layer within a layer of silicon was first realised by Izumi et al in the late 1970s and dubbed SIMOX by them [105]. In this process O\(^+\) ions are implanted at known energies and densities into the silicon substrate. Implantation energies and concentrations in the range 60 to 200 keV and 1.5\(\times\)10\(^{18}\) to 4\(\times\)10\(^{17}\) cm\(^{-2}\) are typical [106–108]. The oxygen concentration as a function of depth gives the profile in figure 3-4(a) [109].

![Figure 3-4: (a) The oxygen concentration profile after the implantation process. Implantation is carried out at 500 to 600 °C. (b) Once annealed there is a well defined boundary between the silicon and buried oxide layer.](image)

During implantation the silicon lattice is damaged by the passage of the oxygen ions. Broken bonds are repaired and the oxide layer formed by annealing at 1350 °C for several hours [106]. Initially the greatest concentration of SiO\(_2\) lies along the line of highest implantation density. This is represented on figure 3-4(a) by the black line where the implantation density \(n_{Ox}\) is a maximum. Any oxygen that finds itself displaced from this region will diffuse towards it due to Ostwald ripening; a process whereby smaller particles merge with larger, more stable bodies [101, 109]. Any dopants within the SOI layer left over from the CZ process diffuse out of this thin layer and into the forming BOX during annealing leaving. This leaves a layer of intrinsic silicon-on-insulator (figure 3-4(b)).

3.4.2 Wafer Bonding and the Smart Cut\(^{TM}\) Process

This method was first proposed by Frye et al [110] and J. Laski [111]. Later in the early 1990s M. Bruel of LETI patented a process that would create thin films of material using the wafer bonding concept [112]. Commercially this became known as the Smart Cut\(^{TM}\) Process and is used heavily in industry.

The wafer bonding process requires two silicon wafers, one is used as a handle wafer and the other becomes host to the SOI layer. These are respectively wafers B and A in figure 3-5. A layer of oxide is grown on the surface of wafer A and will eventually form the buried oxide (figure 3-5(a)). Hydrogen is then implanted through the oxide layer into the silicon to deliberately introduce defects in the crystal structure. This is followed by bonding wafer A to
the surface of the handle wafer (wafer B) (figure 3-5(d)) by heating to 1100 °C. The hydrogen fills vacancies, or bubbles, and exerts a force on the surrounding material when heated. This force is such that a dislocation forms along the implantation line allowing for the mechanical separation of the wafers [101]. A combination of mechanical and chemical polishing (CMP) is used to remove any damage caused by separating the two wafers. Wafer B is then cut off creating the structure in figure 3-4(b).

Figure 3-5: (a) The surface of silicon wafer A is oxidised. (b) Hydrogen is implanted into the wafer. (c) Wafer A is flipped and thermally bonded onto the handle wafer. (d) The system is heated until 'bubbles' (thick dotted black line) form around the implantation region. (e) Wafer A is broken off along the line of defects generated by the implantation and subsequent annealing. The broken section of wafer A can be used again in this process. (f) Any remaining damage from the separation of wafer A is removed with a chemical-mechanical polish. Finally, wafer B is cut off, creating the desired SOI wafer. The rest of B can be recycled.
3.5 Lithographic and Etching Techniques

With the SOI layer formed the silicon mesa must be created by selective covering and etching of the exposed SOI surface. A range of lithographic and etching techniques exist that can be used to achieve the desired mesa dimensions. Two lithographic and two etching techniques are discussed here with the former directly below and the latter in the section after lithography.

3.5.1 Lithographic Techniques

The lithographic processes described here are ultra-violet (UV) photolithography and electron beam (e-beam) lithography. Different sized features can be obtained with either technique with the former allowing for features down to micrometers and the latter tens of nanometers [98]. Although e-beam lithography was considered for use with those samples described in Appendix A, it was ultimately rejected in favour of UV photolithography due to technical considerations of the large feature size and number to be created from the SOI layer.

Ultra-Violet Photolithography

Initially, a viscous photosensitive fluid known as photoresist is spun onto the silicon surface (figure 3-6(a)). The surface of the photoresist is rendered flat by spinning the resist covered silicon at speeds of up to 5000 rpm for 40 to 60 s [98]. Resist thicknesses up to 2.5 µm are common as this ensures the resist will survive later substrate etching. The photoresist is exposed to UV radiation under a photomask opaque to UV in predetermined locations (figure 3-6(b)). Areas exposed to the UV are weakened and then removed by immersing the ensemble in a chemical solution such as 351 solution resulting in the structure in figure 3-6(c). A postbake to remove any excess solvent and harden the resist against subsequent substrate etching is performed at up to 100 °C for 30 to 60 seconds [98]. The selectively exposed regions of silicon are now ready to be etched.

Electron-Beam Lithography

In a similar manner to UV lithography, a viscous fluid known as e-beam resist is spun onto the silicon surface. E-beam resist is, however, sensitive to energetic electrons not UV radiation. As with UV photolithography spinning speeds of up to 5000 rpm for 40 to 60 s are used to create an even, flat surface of e-beam resist [98]. Once spun, the resist is developed by exposure to an energetic beam of electrons. Typical energies range between 10s of eV and 100 keV with higher energies capable of producing smaller features [113, 114]. Once the developed regions of the e-beam resist are removed in developer solution the exposed silicon is ready to be etched.

3.5.2 Etching Techniques

Two methods can be used to etch away material films, these are wet and dry etching and are discussed below.
Dry Etching

Dry etching refers to the use of a plasma hosting an etchant. The plasma will be an ionised noble gas, typically argon, with a source gas mixed in with the plasma. The source gas is chosen according to the material to be etched. For example, carbon tetrachloride (CCl$_4$) etches silicon whilst trifluoromethane (CHF$_3$) etches silicon dioxide [100]. This is used heavily in industry due to the ability to generate an anisotropic etch resulting in well defined, vertical channels. Two common techniques that utilise the above processes are reactive ion etching (RIE) and ion milling, also known as sputter etching. The latter is highly anisotropic as the ions of the noble gas approach the wafer from only one direction. The former can be used to produce narrower features than ion milling which is advantageous where transistor minaturisation is concerned. Once the etch is complete a plasma containing oxygen is used to remove the resist that acted as a protective mask. This is known as ashing [100].

![Diagram](image)

**Figure 3-6:** (a) A cross-section of the resist covered wafer. The substrate has been omitted. (b) A photomask is used to prevent all of the resist being exposed to UV radiation. (c) Any resist exposed to UV is developed in 351 solution. (d) The exposed SOI is removed by immersion in a wet etchant and the beginnings of a mesa are revealed. The remaining resist acts as a mask for the rest of the wafer against the etchant. (e) Finally the resist is removed.

Wet Etching

Wet etching involves the wafer being immersed in a liquid solution. These etches are isotropic in nature which leads to large, potentially undesirable slopes in trench or mesa walls when etching thick materials (figure 3-6(d)). As a result of this isotropy wet etches are used less
frequently in industry than dry etching [100]. Some wet etches are directional in nature and so are used in certain circumstances. For example, potassium hydroxide (KOH) etches the silicon [111] plane more rapidly than either the [110] or [100] planes [115]. The resulting increase in surface area of the silicon has led to this particular etchant being used in the silicon based photovoltaic industry [5]. As with dry etching, the material to be etched determines the etchant used. Silicon can be etched with KOH or, as reported in Appendix A, a solution of ammonium fluoride and nitric acid. Silicon dioxide is typically etched with a buffered oxide etch (BOE) composed of hydrofluoric acid and the buffering agent ammonium fluoride [99]. Once the etch is complete the protective photoresist is removed leaving the structure shown in figure 3-6(e).

3.6 Front Oxide Formation

Having shaped the silicon mesa using lithographic and etching techniques it is now possible to grow the front oxide on the SOI. Here processes are described that enable the growth of a thermal oxide on the SOI layer via chemical vapour deposition (CVD). CVD is discussed first followed by the oxidation methods.

3.6.1 Chemical Vapour Deposition

Although a of number of CVD techniques exist they all rely on the same principles of depositing thin layers of material in gaseous form on a solid substrate surface. Here Low Pressure Chemical Vapour Deposition (LPCVD) is focused upon as it was used to form two important layers in the overall fabrication process. LPCVD, so-called because it is conducted at pressures of between 10 and 10,000 Pa, ensures a homogenous covering of the substrate with the reactants within the source gas [116]. Both the pressure and temperature used depends on both the source gas and target substrate. Here SiO$_2$ was grown on the SOI layer followed by a layer of silicon nitride (Si$_3$N$_4$). Reasons for using these will be explained in the next sections. The source gas for SiO$_2$ is tetraethoxysilane, or TEOS (Si(OC$_2$H$_5$)$_4$). This decomposes on the silicon at a temperature of 700 °C via the reaction [116]

$$\text{Si(OC}_2\text{H}_5\text{)}_4 \rightarrow \text{SiO}_2 + \text{Byproducts}$$

This is used to form a layer of oxide no more that a few nanometres thick. After the SiO$_2$ has been deposited the LPCVD chamber is evacuated of any unwanted byproducts. Silane (SiH$_4$) and ammonia (NH$_2$) are then pumped into the chamber and react on the new silicon dioxide surface at 600 – 660 °C producing the Si$_3$N$_4$ layer [116]

$$3 \text{SiH}_4 + 4 \text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 12 \text{H}_2$$

The processes in which the LPCVD of silicon dioxide and silane are conducted are outlined below.
3.6.2 Oxide Growth

The methods of oxide growth discussed here are front oxide growth and LOCal Oxidation of Silicon (LOCOS). Front oxide growth leads to creation of the front oxide (figure 3-1(a)) and is described directly below. The LOCOS technique allows for the isolation of small regions of the silicon for reasons described below.

LOCOS

The etched SOI layer is prepared for front oxide growth via the LOCOS technique in which specific regions of the SOI are thinned (figure 3-7(f)). This thinning allows for a thicker front oxide to be grown on the SOI layer reducing the parasitic capacitance that would otherwise exist between the gate and the contacts [98].

From an industrial point of view the LOCOS process was developed to insulate MOS transistors from each other on, for example, integrated circuits [98].

Beginning at figure 3-7(a), after the SOI has been defined via lithographic and etching techniques, LPCVD of TEOS is performed producing a few nanometres of silicon dioxide on the SOI (figure 3-7(b)). Further selective oxide growth can be continued once a mask of Si$_3$N$_4$ has been deposited via LPCVD (figures 3-7(c)) and then selectively etched to expose the underlying SiO$_2$ (figure 3-7(d)). An estimable amount of the SOI is converted into silicon dioxide when it is thermally oxidised [117] (figure 3-7(e)). The Si$_3$N$_4$ and thermal oxide are then etched away to expose the selectively shaped SOI as in figure 3-7(f).

Having described the process in full, it will now be explained why the first step of depositing a thin oxide layer as in figure 3-7(b) is necessary. If the process were to be conducted without this thin oxide buffer the Si$_3$N$_4$ would induce strain in the underlying SOI layer during thermal oxidation in figure 3-7(e). This would introduce detrimental defects in the otherwise monocrystalline SOI layer. The strain between the silicon and silicon nitride is greatly reduced by the presence of the oxide buffer as the viscosity of SiO$_2$ at the high temperatures used during thermal oxidation (800 to 1200 °C) lessens considerably [98].
Figure 3-7: (a) The SOI defined via lithographic and etching techniques. (b) A buffer oxide is onto the wafer deposited via LPCVD covering any exposed silicon. (c) A layer of silicon nitride, also deposited by LPCVD, is grown on the buffered oxide. (d) The nitride and oxide are etched away in a series of etches and lithographic processes. (e) A thermal oxide is grown on the exposed SOI. (f) The silicon nitride and oxide are etched away completely.

Front Oxide Formation

Once the silicon has been etched into the desired shape a gate, or field, oxide must be grown on the exposed surface. The most common technique used is thermal oxidation in which either water vapour or molecular (dry) oxygen is pumped into a furnace at 800 to 1200 °C containing the silicon wafer. An oxide forms via a chemical reaction at the silicon surface. For dry oxygen this reaction is [98]

$$\text{Si} + \text{O}_2 \rightarrow \text{SiO}_2$$

while for water vapour

$$\text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2$$

The time $t$ taken to grow a given thickness $X_0$ of oxide on a bare silicon surface is modeled using the Deal-Grove equation [117]

$$t = \frac{X_0^3}{B} + \frac{X_0^2}{B/A}$$  \hspace{1cm} (3.1)
where the ratio $B/A$ is the linear growth rate constant. Some of the silicon is lost to this process, 44% of the oxide thickness will lie below the original surface whilst 56% remains above it [98]. Additionally, due to the conversion of silicon into silicon dioxide, this process can be used to thin the SOI layer.

This process leads to the growth of the FOX in figure 3-8(a).

![Figure 3-8: A schematic cross section of the FOX as it would appear post deposition.](image)

### 3.7 Self-Aligned Front Gate

To create electrical contacts to the SOI the silicon must be doped with either n- or p-type material. These dopants are typically phosphorus or boron where silicon is concerned [98, 100]. Additionally it is a necessity that the gate be aligned with the doped regions such that the contacts do not lie directly underneath or too far removed from the gate. The former case will lead to no current being passed between the source and drain contacts due to the intrinsic volume of silicon lying between the contact and the gate while the latter will mean there are capacitive problems introduced by the contact lying directly below the gate [100]. To create the front gate, silane is deposited over the entire surface of the oxide-covered wafer using LPCVD at 600 °C. At this temperature the silane thermally decomposes on the oxide surface via the reaction

$$\text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2$$

and forms polycrystalline silicon (figure 3-9(a)). Lithographic and etching techniques are then used to mask and remove unwanted regions of the polysilicon exposing the underlying oxide. The new structure is shown schematically in figure 3-9(b).
3.8 Doping Techniques

In order to pass a source-drain current through the device ohmic contacts are required on the SOI surface. There exist a number of ways of achieving this. In the example followed so far ion implantation is used to fire ionised dopants through the oxide layer and into the silicon (figure 3-10(a)); here the front gate acts as a mask for the implantation process. However, the ion implantation damages the silicon as the dopants break bonds and knock silicon atoms out of their lattice positions. To repair this damage and to ensure the dopant atoms fill vacancies within the lattice, the silicon is heated to 1200 °C for one or two seconds via flash heating or laser beam. The short time span activates the dopants (figure 3-10(b)) and ensures any unwanted diffusion is minimised [100]. Although this is a standard industrial technique used in the fabrication of silicon transistors it was well not suited to the procedure described in Appendix A. The silicon MOSFETs experimented upon in Appendix A had oxide interfaces that would have been damaged by such high temperatures.

Other deposition techniques were therefore necessary. Electron beam and thermal evaporation are both methods that require significantly less heating of the silicon in order to drive-in and activate dopants once deposited on the surface of the silicon. In both evaporation techniques the source metal containing the dopant is melted by resistive heating at pressures of roughly $10^{-6}$ mbar [100]. Where thermal evaporation is concerned it is only the thermal diffusion of the material through space to the sample that drives the deposition process. Electron beam evaporation uses an electron beam to eject dopant material from the target crucible onto the silicon. Depending upon the material to be evaporated, the sample is later heated to between 300 to 600 °C to ensure the dopants diffuse into the silicon and take up positions within the lattice. This process is known as drive-in.
3.9 Contact Creation and Passivation

With the silicon doped, photolithographic and metal deposition techniques described above are used to create metal contacts on the sample 3-11(a). Typically aluminium is used and must overlap the doped regions to ensure the silicon underneath the polycrystalline gate can be contacted by the rest of the circuit (figure 3-11(b)). During the fabrication process vacancies in the SOI structure will have formed. These impurities will cause capacitive problems when operating the device if left unchecked. To remove these defects, dangling bonds and fill vacancies a passivation process in which the sample is heated to 500 °C in a nitrogen/hydrogen atmosphere is used [100]. This ultimately results in the final structure shown in 3-11(b) and 3-1(a).

This step was modified in Appendix A.

3.10 Summary

The fabrication processes used in the production of the MOSFETs experimented upon in this study were outlined in this chapter. To summarise, the major steps were the creation of the...
silicon substrate via the CZ method, formation of the SIMOX buried oxide, selective thinning and doping of the SOI, front oxide growth, deposition of the front gate and finally contact metallisation and passivation. Steps relevant to the process described in Appendix A were briefly touched upon and will be discussed in more detail in that chapter.
Chapter 4

The Laboratory

4.1 Introduction

This chapter describes the experimental apparatus used at both room and cryogenic ($T = 2$ K) temperatures. Source-measure units (SMUs) were obtained for applying voltages to the MOSFET gates and source-drain contacts. These SMUs were also used to measure the resulting currents at both the gates and source-drain contacts. The SMUs were connected to the MOSFET via a number of switchboxes made by the author. MOSFET temperature was controlled by a helium cryostat that enabled temperatures of 2 K to be attained. The magnet within the cryostat allowed for Hall measurements to be conducted at low temperatures. Additionally, Hall measurements were made at room temperature using a resistive magnet. The SMUs and resistive magnet were all controlled using LabVIEW software. The code itself is described in this chapter while a full presentation of it can be found in Appendix B.

Although most of the experimental work was conducted at The University of Bath a number of important experiments were carried out at the high magnetic field laboratory in Grenoble and at the Nippon Telegraph and Telephone (NTT) Corporation in Japan. The nature of these experiments is detailed here as data from those experiments appears in later chapters.

4.2 Initial Measurements

Experiments were initially conducted at room temperature as no suitable equipment was available for low temperature measurements. It was also simpler, from an experimental point of view, to test a sample before cooling to determine whether the device possessed any shortcircuits that would render it unusable. When applying a source-drain voltage to either an n- or p-type contact either alternating or direct current, AC and DC respectively, would be used. The phase of the AC data allowed a check for any capacitive problems in the circuit. Unless otherwise stated all of the SMUs were controlled and data collected via a LabVIEW program on a PC. A schematic diagram of this program can be found in Appendix B.
A photograph of the apparatus used for room temperature measurements at Bath University is shown in 4-1. Model numbers and names for the different Agilent and Keithley SMUs are given in figures 4-1(a) and (b). Each performed a specific task based on the voltages each SMU was capable of applying. As the Keithleys possessed the greatest voltage-current measurement range, ±200 V, they were used for applying back gate voltages of up to ±50 V [118]. Additionally, the Keithleys were used to apply direct source-drain voltages and measure source-drain currents as they could measure accurately to $10^{-11}$ A [118]. The Agilent U2722A was used only for applying front gate voltages as its operating range was ±20 V [119]. The lock-in amplifiers (figure 4-1(c)) were used for applying alternating voltages to the source and drain and measuring the corresponding AC. Typically a voltage sensitivity in the range 3 V to 1 mV was used; however, the lock-ins were capable of sensitivities of 3 V to 10 nV [120]. All of the previously described SMUs could be connected to the PC via GPIB cables allowing each to be controlled by the LabVIEW program. The only SMU unable to be remotely operated in this manner was the Agilent E612A (figure 4-1(b)). This meant that data could not be readily collected from this SMU and so it was used only to apply front or back gate voltages in the ranges ±15 V and ±50 V respectively. Figure 4-1(e) shows the liquid nitrogen cryostat. Ultimately it was not used due to an internal leak that meant nitrogen could escape leading to premature heating of the sample. Despite this, the author used the wiring of the nitrogen insert as practise for wiring the helium cryostat’s insert. The resistive magnet (figure 4-1(f)) was used to perform Hall measurements as described in Chapter 2.

Figure 4-1: (a) The BNC switchbox through which the SMUs were connected to the sample (b) From left to right, the Agilent U2722A, a Keithley 2400 and the Agilent E612A (c) The two 5210 lock-in amplifiers. (d) The control unit for the resistive magnet. (e) The liquid nitrogen cryostat. (f) The resistive magnet and water cooling system supply pipes located on the wall.

Gluing the sample onto a chip carrier using conducting silver paste (figure 4-2(a)) and securing the chip carrier within the sample box in figure 4-2(b) ensured the MOSFET was stable and perpendicular to the magnetic field. The device was positioned deliberately so that it lay within a region of uniform magnetic field.
The BNC switch box in figure 4-1(a) enabled each aluminium contact on the MOSFET to be connected to an SMU or grounded separately. When connecting an SMU to some contact on the MOSFET the relevant switch on the BNC array would be left in the up position. To ground that contact without first disconnecting the SMU required only that the user push the switch to the down position.

The next section describes the use of the SMUs and resistive magnet in AC and DC experiments.

4.2.1 AC and DC Experiments

Figures 4-3(a) and (b) show schematic setups respectively for DC and AC setups. In a typical DC measurement the Agilent U2722A would apply a front gate voltage that continuously changed between $-15$ V and $+15$ V. Simultaneously a Keithley would apply a constant source-drain voltage and measure the source drain current as a function of the changing gate voltage. Either another Keithley or the Agilent E612A would apply a constant back gate voltage for the duration of the front gate voltage sweep. This back gate voltage would lie in the range $\pm 50$ V. As the Agilent E612A could not be remotely controlled via the LabVIEW program it would only be used if no other SMU were available. If Hall measurements were being made then the MOSFET would be placed between the poles of the magnet and the magnetic field swept between $\pm 1$ T for a constant set of gate voltages applied by the Agilent U2722A and a Keithley or the other Agilent. Simultaneously a Keithley would be used to apply a constant source-drain voltage of 10 mV while the lock-in amplifiers measured $V_{xy}$ and $V_{xx}$. The data collected in this way would be used to calculate carrier densities as described in Chapter 2.

For AC measurements without a similar process as described for DC measurements repeated but using the lock-ins to apply an oscillating source-drain voltage in place of the Keithley. This is shown schematically in figure 4-3(b).

An additional measurement that was performed using an oscillating source-drain voltage was one in which the current applied through the device was limited by a large load. Here a lock-in would apply the oscillating voltage. Between the output of the lock-in and the source-drain voltage was a 10 M$\Omega$ resistor. This setup limited the current that could be drawn through the
device and was used when a sample was found to be working yet showed signs of a shortcircuit above a certain current threshold.

![Diagram](image)

Figure 4-3: (a) DC setup. (b) AC setup. Lock-in 1, applying the alternating source-drain voltage ($V_{OSC}$), acted as the reference for lock-in 2. The ground of lock-in 1 ($V_{GND}$) was connected to the drain contact to complete the electronic circuit. Voltages $V_{xx}$ and $V_{xy}$ were measured using probes A and B on lock-in.

Table 4.1 summarises the equipment used for experiments. The full device name, number of devices used in a given experiment and their application are listed therein.
<table>
<thead>
<tr>
<th>Device</th>
<th>Number used</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Keithley 2400</td>
<td>3</td>
<td>Applying DC source-drain voltages and measuring the resulting current. Applying back gate voltages. Measuring inter-layer currents between the front and back oxide interfaces.</td>
</tr>
<tr>
<td>Agilent U2722A</td>
<td>1</td>
<td>Applying front gate voltages.</td>
</tr>
<tr>
<td>Agilent E612A</td>
<td>1</td>
<td>Applying back gate voltages.</td>
</tr>
<tr>
<td>The lock-in amplifiers</td>
<td>2</td>
<td>Applying AC source-drain voltages and measuring the resulting current. Measuring $V_{xx}$ and $V_{xy}$.</td>
</tr>
<tr>
<td>Resistive magnet</td>
<td>1</td>
<td>Used to determine carrier densities at room temperature.</td>
</tr>
</tbody>
</table>

Table 4.1: SMUs used at room temperature.
4.3 Cryogenic Temperatures

This section is concerned primarily with the operation of the helium cryostat itself as the experimental setup of the SMUs was virtually identical to that used at room temperatures. Most of the SMUs that were used for room temperature measurements were also used for cryogenic experiments. The Keithleys, Agilents and lock-ins are shown in figures 4-4(a). A simple schematic of the experimental setup at cryogenic temperatures can be obtained by replacing the resistive magnet in figures 4-3(a) and (b) with the magnet in the cryostat and the sample box in the same figures with the variable temperature insert.

![Image](image_url)

Figure 4-4: (a) The upper three levels of the rack contain the lock-in amplifiers, Keithleys and Agilents shown in 4-1. Another BNC switchbox was created specifically for this arrangement. (b) The superconducting magnet controller used to apply a field of up to 7 T to the sample. (c) Temperature display for the insert (left) and the liquid helium depth monitor (right). (d) Helium cylinder used in the helium transfer process. (e) The helium cryostat. (f) An Edwards 5 pump that could pump on either the variable temperature insert or the liquid helium itself.

The helium cryostat was obtained from ICEoxford (Innovative Cryogenic Engineering) (figure 4-4(e)). Other components that were supplied with it included the superconducting magnet controller (figure4-4(b)), the temperature display unit (figure4-4(c)) and the liquid helium depth monitor (figure4-4(c) to the right of the temperature display unit). The two final components that were supplied by ICEoxford were the Variable Temperature Insert (VTI) and the insert on which the sample would be secured. These are shown in figures 4-5(b) and (a) respectively. The insets in figure 4-5 show plan and side views of the sample holder. This ensemble was screwed onto the tip of the insert.
To cool the cryostat to cryogenic temperatures a pre-cool would initially be carried out by pouring liquid nitrogen into the main bath of the cryostat (figure 4-6(i)) via the port for the VTI (figures 4-6(d) and 4-8(a)(iii)) until it covered the magnet. The nitrogen level was checked using both the depth monitor and by eye. Pre-cooling lowered the temperature to 77 K and in doing so removed a large amount of the thermal energy within the system without wasting the more expensive liquid helium. The temperature within the main bath was monitored by measuring the resistivity of the electromagnet with a digital multimeter. As the temperature of the magnet dropped the resistivity also decreased until eventually it became low and constant. The nitrogen would then be removed by pressurising the main bath with helium gas from the cylinder in figure 4-4(d). The main bath, now empty, had liquid helium transferred to it from a helium containing Dewar pressurised by the helium cylinder 4-4(f). Simultaneously the sample would be affixed to the insert (figure 4-5(a)) and the insert loaded into the VTI (figure 4-5(b)).
Figure 4-6: Schematic cross-section of the cryostat. (a) Sample wiring. (b) The variable temperature insert. (c) The insert (d) Liquid helium transfer point. (e) Pipe connecting the VTI to the Edwards pump. (f) Over pressure port and valve. (g) The radiation baffles within the vacuity of the main body of the cryostat. (h) The insert tip and sample space. (i) The electromagnet in the main bath. The helium must be at least as high as the dotted line in order to safely operate the magnet. (j) The valve between the sample space and the main bath.

Initially the needle valve (figure 4-6(j)) separating the sample space and main bath was left closed to prevent helium in the main bath being lost to the 'pump and purge' process the VTI was subjected to. This process was conducted by purging the VTI of air by allowing helium gas from the main bath into the sample space and then pumping on the VTI by opening valve 1 and ensuring valve 2 was closed (figure 4-7). Valve 1 would then be closed and valve 2 opened
to allow helium from the main bath into the VTI. Valve 2 would then be closed again and valve 1 opened. This process was repeated at least 5 times to ensure that any oxygen or nitrogen present in the VTI was removed. If these gases were present in the VTI during cooling they would condense and in doing so detrimentally affect the cooling rate of the sample space when helium was later allowed into that volume.

Figure 4-7: Schematic diagram of the pump system. To pump and purge valve 2 would be left open and valve one closed. After waiting for 30 seconds valve 2 would be closed, valve one opened and the pump switched on. This would evacuate the VTI of any helium and/or air. This process would be repeated a number of times to ensure all the air had been removed.

With the pump and purge process complete the needle valve would be opened using the knob shown in figure 4-8(b)(iv). Pumping on the VTI with the valve open cooled the sample as cold helium gas drawn from the main bath rushed past the sample itself. This process accelerated as the VTI was slowly lowered to its final position shown in figure 4-8(b). During operation it was found that opening the needle valve to between 10 and 11 on the valve’s unitless scale provided a controllable decrease in the temperature. If there were no pumping action then the sample space would reach thermal equilibrium with the main bath and maintain a constant temperature of 4.2 K. To cool the sample below 4.2 K required the VTI to be pumped on continuously. This produced a pressure difference between the atmospherically pressurised main bath and the lower pressure sample space. The lower pressure in the VTI lead to a reduction in the temperature at which the liquid attained phase equilibrium with its surroundings, allowing the liquid helium to attain a lower temperature of 1.8 K in the sample space. The cryostat was capable of maintaining this base temperature for a number of days without needing a top-up of helium due to both the vacuum surrounding the main bath and VTI and the insulation within the VTI. The insulation contained activated charcoal and pumped on its surroundings.
Figure 4-8: (a) and (b) are respectively the top of the cryostat without and with the VTI loaded. (a)(i) The pump port connected to the Edwards pump and over-pressure valve. (ii) Wiring for the helium depth monitor. (iii) VTI loading port - shown closed. (iv) Magnet diagnostic wiring. (v) Helium transfer pipe - shown closed. (vi) Current carrying leads to the magnet. (b)(i) Wiring for the temperature probe in the sample space. (ii) Wiring from the sample to the BNC array and SMUs. (iii) VTI diagnostic wiring. (iv) Needle valve. (v) Pressure relief valve.

Once cooled experiments would begin in earnest so as to ensure as little helium was wasted as possible. Experiments were typically conducted within a temperature range of 1.7 to 6 K - the exact value was controlled by careful manipulation of the needle valve. When the magnetic field was used, the maximum operating field strength of 7 T was used to ensure clear Shubnikov-de-Haas oscillations were observed.

The next three sections describe experiments conducted elsewhere besides the University
of Bath. Work performed at these locations is presented in later chapters. The LabVIEW program is also described in the penultimate section of the chapter.

4.4 Grenoble

Experiments at the high magnetic field laboratory at the CNRS in Grenoble took place in June 2012. A 30 T electromagnet, cooled by water from the nearby river Drac, contained within it a helium cryostat. This ensemble was embedded in the floor of the laboratory. Experiments described in previous sections in this chapter were conducted with similar equipment to that used in Bath. Gate voltages were applied with Keithley SMUs while lock-in amplifiers were used to apply a source-drain voltage and simultaneously measure \( V_{xx} \) and \( V_{xy} \). The temperature of these experiments was varied between 1.7 K and 6 K by means already described in this chapter. Chapters 6 and 8 detail the results from these experiments.

4.5 The Nippon Telegraph and Telephone Corporation

The work conducted at NTT used samples that, unlike the rest of those detailed in this work, were not Hall bars. They still had the structure shown in in figure 3-1(a) but were host to different contact layouts. The samples were left uncleaved in the wafers on which they were produced to minimise the chances of damaging the devices. This meant that a probe station had to be used to reach the source-drain and gate contacts. The metal plate upon which the wafers rested was used as the back gate contact. Measurements were conducted at 6 K and at pressures of \( \approx 10^{-7} \) Atmospheres. This pressure was attained by use of a diffusion pump to achieve \( \approx 10^{-5} \) Atmospheres before a molecular turbo pump was activated, further reducing the pressure. The temperature was lowered by use of a liquid helium based refrigeration system. These experiments are discussed in chapter 9.

4.6 The LabVIEW Program

The 'code' for LabVIEW does not appear in this thesis as, although such a thing exists, it would be extremely unwieldy to try to display and explain. All LabVIEW programs are split into two major parts - the front panel and the block diagram. The latter is where the 'code', or objects, is entered. An annotated example of one of the block diagrams used for this work appears in Appendix B. Objects can be anything from drivers that communicate with the SMUs to mathematical formula or even C-code. Once placed, relevant inputs appear on the front panel. It is these inputs that the experimentalist uses to set voltages and measure currents with the SMUs. LabVIEW was used as it allows easy communication and timing between apparatus of different suppliers with a simple method of outputting data. Although a number of programs were written, ultimately only two were used regularly. The first permitted the experimentalist the option of controlling the resistive magnet along with two Keithleys, the Agilent U2722A
and lock-ins. The second allowed for the control of up to three Keithley and the lock-ins. Both programs allowed the user to set voltages for the SMUs to apply and measure the resulting current. For example, the second program could be set so that SMU 1 applied a constant source-drain voltage while measuring the current as a function of a gate voltage applied by SMU 2. Once SMU 2 had finished a sweep it would reset back to its original value or 0 V if the user so desired. A third SMU could be used to apply a back gate voltage that changed whenever the second SMU finished its sweep. Once all voltages had attained their final, user set values, the program ramped all SMUs to 0 V. In this way an experiment could be left running obtaining data over the course of a weekend or longer if deemed necessary. It is data obtained via the use of these programs that appears in Chapters 5 and Appendix A.

4.7 Chapter Summary

In this chapter the room and cryogenic temperature experimental setups used throughout the rest of this work were detailed. The operation of the helium cryostat was explained at length. Experiments conducted in both Grenoble and NTT were described with data obtained at those locations appearing in chapters 8 and 9 respectively.
Chapter 5

Current-Voltage Characteristics of a Vertically Coupled Electron-Hole System

5.1 Introduction

In this chapter the drastic changes to the I-V characteristics of a 2D electron (2DEG) in the presence of a 2D hole gas (2DHG) within the SOI layer are demonstrated at room temperature. Gate voltages over which an electron-hole bilayer is present within the quantum well are identified at low source-drain voltages of 10 mV. The effects of applying a large source drain voltage (±1 V) on the I-V characteristics of a 2DEG (2DHG) type in the presence of the other carrier type are described as a function of carrier density. The results are explained using a textbook model that is initially used to describe the single layer I-V characteristics [51]. This model is then extended to describe the I-V characteristics of a single layer in a bilayer system. Under certain conditions a current could be passed between the electrons and holes despite their physical separation. The penultimate section of this chapter deals with this inter-layer current and a qualitative model is proposed for its origin.

5.2 Background and Chapter Overview

The physics underlying the electronic transport properties of single layers of two-dimensional (2D) electrons or holes has been studied for many decades in a wide range of semiconducting systems as described in Chapter 1 [47, 48, 51]. Additionally, with the advent of transistors with two gates, systems with two spatially close, electrically isolated 2D charge carrier systems began to be investigated [10]. Theoretical predictions about the nature of these bilayer systems revealed the possibility of new physics arising due to the intimacy of the layers [121]. Fundamental physics pertaining to interlayer interactions have indeed been revealed in the study of
bilayers [10, 11, 122–126]. However, despite the numerous studies on bilayers, the basic transport properties of a 2DEG or 2DHG in the presence of the other 2D carrier gas over a wide range of gate and source-drain voltages remains understudied.

There are two reasons for this, one being the fragility of the devices hosting the bilayer system as the insulating layers present in the samples risk breaking down if too great a bias is applied to the source-drain or gate contacts. As sample creation is time intensive and potentially expensive, the experimentalist may not want to risk damage to, or the destruction of, their devices. The second reason relates to the relationship between the applied voltage and the source-drain current. For low voltages (10 - 100 mV) the current responds linearly and is thus readily modeled. The few studies that do investigate the effect of one 2D carrier gas on another restrict themselves to low temperatures and/or constant source-drain biases [55, 126].

In this chapter source drain voltages of ±1 V are applied to the n- and p-type contacts of a Si-MOSFET over a wide range of gate voltages at room temperature. The gate voltages used permitted a large variation in the carrier density which allowed for a density-based interpretation of the source-drain current and conductance characteristics at large source-drain voltages. The rest of the chapter is split into three parts. The first details the methods used to generate an electron-hole bilayer in the SOI layer of the MOSFET at low source drain voltages (10 mV). Additionally, carrier densities are measured when a single or bilayer system is present within the SOI quantum well. The second part describes the model used to fit experimental conductance data obtained at large source-drain voltages (±1 V). The third part examines the origin of the inter-layer current that flows between the electrons and holes for certain values of the source-drain voltage.

5.3 Low Source-Drain Voltages

Here the source-drain current of the electrons and holes is measured over a wide range of gate voltages. This enabled the regions of carrier coexistence to be identified. Carrier densities were measured using techniques described in Chapters 2 and 4 allowing for the dependence of the source-drain current and source-drain conductance data to be interpreted in terms the carrier density of each 2D layer. Details of the capacitance calculations and explanation of the method used to extract threshold voltages are also described here as they will be used in later sections.

5.3.1 Identifying Electron-Hole Coexistence within the Silicon Quantum Well

As described in Chapter 2, applying a gate voltage bends the conduction or valence in the SOI layer. When the Fermi level $E_F$ lies within either the inversion or accumulation layer generated by the applied voltage some density of electrons or holes, respectively, will be present in the system [51]. Figure 5-1 shows this schematically where figures 5-1(i) and (ii) correspond to the case where the quantum well is symmetric and only electrons or holes are present within the
quantum well respectively. The lines of zero electron \((n_e)\) or hole \((n_h)\) density enclose regions where the source-drain voltage is zero. For the electrons this corresponds to negative gate voltages that deplete the electrons from the quantum well and prevent conduction through the system. A similar region exists for the holes for positive gate voltages above the red line. The ‘diamond’ in the centre of figure 5-1 enclosed by the \(n_{e,h}\) lines is a region in which the quantum well is completely devoid of electrons and holes. Conversely, the areas in the upper left and lower right of figure 5-1 correspond to where both electrons and holes exist simultaneously within the well; note that the red and blue lines are guides to the eye. Within these regions, the Fermi level crosses both the valence and conduction bands and an electron hole bilayer is present within the quantum well (figures 5-1(iii) and (iv)). As these are the regions of interest in this section and Chapter they are described further below before the experimental data demonstrating the presence of a bilayer is presented.

![Figure 5-1: Lines where the electron (blue) and hole (red) density is zero; these lines are guides to the eye. The line of symmetry is the line along which the quantum well is symmetric with gate voltage. (i) The Fermi level lies at the bottom of the flat conduction band at this point. (ii) Here the top of the valence band has just been occupied. (iii) and (iv) are the gate voltages at which the Fermi level just crosses both the conduction and valence band edges.](image)

These regions of carrier coexistence are considered in further detail in figures 5-2(a)(i) to (a)(iv). At gate voltages where a bilayer is present, the electric field in the quantum well is given by \(F = E_G/d\) (figure 5-2(a)(i)). Under these conditions the Fermi level \(E_F\) exists in both the conduction and valence bands and at the same time (figures 5-2(a)(ii) and (iii)) [126].

65
Figure 5-2: From [126]; $E_e$ and $E_h$ are the electron and hole subbands respectively. (a)(i) and (ii) Shape of the quantum well required to obtain coexistence without (i) and with (ii) quantum confinement. (iii) As (ii) but with the gate potentials reversed. (iv) As (iii) but with a potential bias applied to the holes. (b)(i) and (ii) Schematics of the experimental setup for both the electron and holes with n- and p-type contacts shown.

Gate voltages for which an electron-hole bilayer was present within the SOI layer were determined by applying 10 mV to an n- or p-type contact (figures 5-2(b)(i) and (b)(ii)) and measuring the source-drain current as a function of front and back gate voltages; $V_F$ and $V_B$ respectively. The results for the electrons and holes are shown in figures 5-3(a) and (b). For both carrier types the electron or hole current is large when the gate voltages are of opposite sign to the electron or hole charge. These gate voltages correspond to figure 5-1(i) for the electrons and 5-1(ii) for the holes. At large gate voltages of opposite sign ($V_B \approx \pm 36$ V, $V_F \approx \pm 7.5$ V) the source-drain current for both carriers is non-zero. This is indicative of an electron-hole bilayer occupying the SOI layer as also found by Takashina et al. and Prunnila et al. [11, 126]. These areas can be found in figures 5-1(iii) for the electrons and 5-1(iv).
Figure 5-3: (a) and (b) are the electron and hole current respectively as a function of front and back gate voltage.

It was in these regions where the electron and hole currents, $I_e$ and $I_h$ respectively, were simultaneously non-zero that experiments to determine the effect of one carrier type on the other’s I-V characteristics were conducted. Different effects were found depending upon the density of both the electrons and holes. The dependence of the electron and hole densities on gate voltages at source-drain voltages of 10 mV is described in the next section.

### 5.3.2 Carrier Densities

Electron and hole densities are determined over a wide range of gate voltages in this section. The trends with front and back gate voltage of the carrier densities are then used to calculate capacitances and threshold voltages of the system. The capacitances and threshold voltages are used later when modeling the I-V characteristics of the carriers at larger source-drain voltages.

Densities of the electrons and holes, $n_e$ and $n_h$ respectively, were found via Hall measurements using a resistive magnet as described in Chapter 4. The magnetic field was applied at right angles to the sample; perpendicularity was enforced by the sample being secured in the sample box (figure 4-2(b)) between the poles of the magnet. Figures 5-4(a) and (b) show data for the electrons and holes respectively at high and low densities. The gate voltages used to set these densities were such that only electrons or holes were present in the quantum well. The
variation in the $R_{xy}$ signal at lower densities was caused by $R_{xx}$ being comparable in size to the $R_{xy}$ signal. When a bilayer was present in the quantum well, the Hall voltage would only be measured in the charge layer to which a source-drain voltages was being applied. For example, if a source-drain voltage were applied to the 2DEG, only the Hall voltage in the electron layer would be measured. The 2DHG would be grounded and was assumed to have no effect on the electron Hall voltage.

Figure 5-4: (a) and (b) respectively the electron and hole dependence of $R_{xy}$ on out of plane magnetic field. The red lines are examples of fits to the data at lower densities.

Using equation 2.11 the electron and hole densities were calculated and plotted as a function of gate voltage. Some examples of the dependence of carrier density on gate voltage are shown in figures 5-5(a) to (d). Not all the data obtained is shown for reasons of clarity. For gate voltages where only a single, 2D layer of carriers was present within the quantum well a linear dependence of the density on gate voltage can be observed. A deviation from this straight line behaviour can be observed for large gate voltages where the density saturates and becomes constant. This can be explained by considering the following. When a large positive back gate voltage has been applied to the device as in figure 5-5(a) and $V_F = 0$ V the electron density at the BOX/SOI interface is non-zero. Applying a negative front gate voltage depletes the electrons and reduces their density. As $V_F$ is made more negative, the hole density at the FOX/SOI interface increases from zero to some value capable of screening the electrons from the depleting effects of the back gate [11, 126]. This screening halts the observed decrease in electron density in figure 5-5(a). Similar reasoning can be applied to figures 5-5(b) to (d), although the carriers being screened may be at the FOX/SOI interface instead. Additionally, there is a deviation from the linear dependence of carrier density on gate voltage as $V_F$ and $V_B$ pass through 0 V. This is caused by the occupation of the upper spatial subband, or alternatively, when the carrier density at both FOX and BOX/SOI interfaces are simultaneously non-zero. The presence of these carriers changes the capacitance of the system and its effects in figures 5-5(a) to (d) can be observed as a change in gradient [126]. These figures were used to calculate capacitances between the gates and the single carrier systems as demonstrated below.
Figure 5-5: (a) and (b): Electron density as a function of front and back gate voltages for instances where the electrons were at the front or back SOI/oxide interfaces. Capacitances were calculated away from the regions of coexistence. (c) and (d): As per the electrons but for the holes.

5.4 The Two Cases

Here the 2 Cases introduced in the previous section are expanded as clarifying the two scenarios will aid explanation of both the I-V characteristics and the inter-layer current in later sections.

Experimentally, a source-drain voltage would be applied to the electrons or holes and the source-drain current measured. When considering the effects of gate voltage on the carriers, it was important to be clear about which interface the carriers were closest to as this had ramifications for the capacitance between the carriers and the gates; as shown in the previous section. The two Cases were used to reduce confusion when discussing the experimental data; this becomes especially pertinent when the inter-layer current is later considered. In Case 1 the electrons were closest to the SOI/FOX (front) interface while the holes were closest to the SOI/BOX (back) interface (figure 5-1(iv)). Conversely, in Case 2, the electrons were closest to the back and the holes closest to the front (figure 5-1(iii)). The experimental setup corresponding to Cases 1 and 2 is shown in figure 5-6(a) and (b) respectively. In figure 5-6(a) the source-drain voltage was applied to the electrons at the front or the holes at the back. In figure 5-6(b) the source-drain voltage was applied to the electrons at the back or the holes at the front. For both Cases the inter-layer current is referred to as $I_{eh}$ or $I_{he}$ to distinguish which carrier layer the interlayer current was flowing. $I_{eh}$ refers to the source-drain voltage being applied to the electrons and a current being measured at the p-type contact. Conversely, $I_{he}$
refers to the setup whereby the source-drain voltage was applied to the holes and a current measured through the n-type contact.

Figure 5-6: Case 1 corresponds to (a) while (b) is to Case 2. In both, a voltage $V_{e,h}$ is applied to a given carrier type and $I_{e,h}$ measured. When $V_e$ is applied any current $I_{eh}$ through the 2DHG is monitored for. When $V_h$ is applied any current through the 2DEG ($I_{he}$) is measured.

5.5 Capacitances and Threshold Voltages

Here the methods used to determine the capacitances and threshold voltages when a single carrier type occupies the quantum well are described. These values will be used in the model applied to the data at large source-drain voltages.

5.5.1 The Capacitances

To determine the capacitances between the gates and a given carrier type, the gradients of the lines in figures 5-5(a) to (d) were used in the equation [11, 51]

$$C_{F,B} = \pm e \frac{\partial n_{e,h}}{\partial V_{F,B}}$$  \hspace{1cm} (5.1)

where $C_{F,B}$ is the capacitance from the front or back gate to the electrons or holes. Only the linear regions in figures 5-5(a) to (d) away from areas where a bilayer was present were used in calculations. For each carrier type, two values of $C_F$ and $C_B$ would be calculated for the following reasons. In figure 5-3(a) the single layer of electrons, for example, could be either closest to the FOX/SOI interface at negative $V_B$ and positive $V_F$ or they could be closer to the BOX/SOI interface for positive $V_B$ and negative $V_F$. A similar situation is also true for the holes, however, when a negative $V_B$ and positive $V_F$ are applied, the holes were closest to the BOX/SOI interface whilst for positive $V_B$ and negative $V_F$ they were closest to the FOX/SOI interface. The different positions the carriers could occupy within the well lead to the change in capacitance with respect to either gate. To avoid confusion in later sections of this Chapter the following cases were defined. Case 1 corresponds to the situation where the electrons were closest to the FOX/SOI interface while the holes were closest to the BOX/SOI interface. Conversely, Case 2 was when the holes were closest to the FOX/SOI interface while the electrons
were closest to the BOX/SOI interface; these two cases are discussed later. Capacitances for both cases are shown in table 5.1.

<table>
<thead>
<tr>
<th>Case</th>
<th>Carrier Type</th>
<th>( C_F ) (( \mu \text{Fm}^{-2} ))</th>
<th>( C_B ) (( \mu \text{Fm}^{-2} ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Electrons</td>
<td>430 ± 4</td>
<td>94</td>
</tr>
<tr>
<td></td>
<td>Holes</td>
<td>364 ± 2</td>
<td>92 ± 1</td>
</tr>
<tr>
<td>2</td>
<td>Electrons</td>
<td>365 ± 4</td>
<td>93</td>
</tr>
<tr>
<td></td>
<td>Holes</td>
<td>429 ± 4</td>
<td>90</td>
</tr>
</tbody>
</table>

Table 5.1: Front and back capacitances for both Cases.

These capacitances are compared with the nominal values \( C_{\text{FOX}} \) and \( C_{\text{BOX}} \) in table 5.2. These correspond to where the 2DEG or 2DHG was present at either interface. The equation used for this was \( C = \epsilon_0 \epsilon_r / d \) where \( \epsilon_0 \) is the permittivity of free space, \( \epsilon_r \) the relative permittivity of the silicon in the quantum well or the oxide layers and \( d \) the thickness of the different layers. Nominal thicknesses of the FOX, SOI and BOX were 81 ± 1 nm, 40 ± 1 nm and 380 ± 1 nm respectively.

<table>
<thead>
<tr>
<th>Carrier position (Interface)</th>
<th>( C_F ) (( \mu \text{Fm}^{-2} ))</th>
<th>( C_B ) (( \mu \text{Fm}^{-2} ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>FOX/SOI</td>
<td>426 ± 4</td>
<td>88</td>
</tr>
<tr>
<td>BOX/SOI</td>
<td>367 ± 3</td>
<td>91</td>
</tr>
</tbody>
</table>

Table 5.2: Nominal front and back capacitances.

The capacitances in table 5.2 agree to within the experimental errors of those values in table 5.1.

5.5.2 The Threshold Voltages

The threshold voltages are not uniquely defined quantities. For example, the front gate voltage required to observe a non-zero carrier density at the front interface differs depending upon the back gate voltage. Here they are defined as being the minimum voltage required to obtain a non-zero density in either the conduction or valence bands when the electric field in the quantum well is zero. These points lie at the intersection of the \( n_c = 0 \text{ m}^{-2} \) and \( n_h = 0 \text{ m}^{-2} \) lines with the line of symmetry in figure 5-1. Calculating the \( n_c = 0 \text{ m}^{-2} \) and \( n_h = 0 \text{ m}^{-2} \) lines required the extrapolation of the data in figure 5-5 to \( n = 0 \text{ m}^{-2} \). This produced a pair of gate voltages for which that particular carrier density was zero. These 'voltage coordinates' were then plotted on the \( (V_F, V_B) \) plane (figure 5-7). In this way straight lines were plotted and then extrapolated until they intersected with the symmetry line, also shown on figure 5-7. The errors in the \( n = 0 \text{ m}^{-2} \) points were used to create a range over which the extrapolated line could intercept the symmetry line. This resulted in a range of values that the threshold voltages could take.
Table 5.3 shows the threshold voltages for the electrons and holes and the errors associated with those values. Although the errors in the threshold voltages were large this was thought to be of minimal consequence when modeling the I-V data was concerned for reasons given when forming the model in later sections.

<table>
<thead>
<tr>
<th>Carrier Type</th>
<th>$V_{Th}^e$ (V)</th>
<th>$V_{Th}^h$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrons</td>
<td>$-0.25 \pm 0.10$</td>
<td>$-1.20 \pm 0.49$</td>
</tr>
<tr>
<td>Holes</td>
<td>$-0.55 \pm 0.10$</td>
<td>$-2.60 \pm 0.46$</td>
</tr>
</tbody>
</table>

Table 5.3: Threshold voltages.

5.6 Large Source-Drain Voltages

The density data obtained at a source-drain voltage of 10 mV was used as a foundation for the model presented in this section. The model is described in detail, beginning with a textbook equation used to describe the G-V data when only a single carrier type was present in the quantum well. The model is then extended to describing the G-V characteristics of a single carrier layer in a bilayer system. That data is then presented for both Cases 1 and 2 and the model applied to it.

5.6.1 The Model

A textbook model was initially used to fit regions of the data where only a single 2DCG was present in the silicon quantum well. This was extended to the case where both a 2DEG and
2DHG were present in the quantum well. The assumptions underlying the use and extension of the textbook model are outlined and discussed in this section. The capacitances and threshold voltages determined in earlier sections are applied here and the reasons for accepting a large error in the threshold voltages explained.

A Single 2DCG

The behaviour of the source-drain current as a function of source-drain voltage required first understanding the behaviour of a single 2DEG or 2DHG in the silicon quantum well. This allowed for a foundation to be made from which the model could be later extended. The textbook model was used for this was [51]

\[ I_{e,h} = g \mu_{e,h} \left( V_{e,h} \left( (V_F - V_{Th}^F)C_F + (V_B - V_{Th}^B)C_B \right) - \frac{V_{e,h}^2}{2} (C_F + C_B) \right) \]  (5.2)

and the differential conductance \( G_{e,h} = dI_{e,h}/dV_{e,h} \) is given by

\[ G_{e,h} = g \mu_{e,h} \left( ( (V_F - V_{Th}^F)C_F + (V_B - V_{Th}^B)C_B) - V_{e,h}(C_F + C_B) \right) \]  (5.3)

where \( g \) is the geometric factor of the Hall bar, \( \mu_{e,h} \) is the electron (hole) mobility, \( C_F \) and \( C_B \) are the front and back capacitances respectively and \( V_{Th}^F \) and \( V_{Th}^B \) are respectively the front and back threshold voltages. The capacitances and threshold voltages in tables 5.1 and 5.3 would be used in equation 5.3 when fitting the data. The gradients in figures 5-5(a) to (d) do not change significantly over a range of gate voltages where only a single 2D carrier gas (2DCG) was present within the quantum well. From this it was assumed that \( C_F \) and \( C_B \) also remained constant over the same gate voltages.

For low source-drain voltages the only contribution to the carrier density originated from the gate voltages. For large source-drain voltages the density of the carrier gas was affected by the source-drain voltage as the effective gate voltages \( V_{eff}^{F,B} \) applied to the carrier gas became \( V_{eff}^F = V_F - V_{e,h} \) and \( V_{eff}^B = V_B - V_{e,h} \). So for a constant set of gate voltages, the only further contribution to the carrier density came from the change in the applied source-drain voltage. As the capacitances and gate voltages were constant for a given G-V trace, the carrier mobility was used as the sole fitting factor in equation 5.3. The intercept of equation 5.3 was given by the density of the carriers at \( V_{e,h} = 0 \) V while the gradient was governed by the carrier mobility. Only the mobility governs the gradient of the G-V graphs so the fact that the errors in the intercepts were so large was of minimal consequence as they were not the quantities under consideration. It was assumed that the carrier mobility remained constant across the \( V_{e,h} \) range used. It was also assumed that for a given front gate voltage the mobility did not change significantly for the back gate voltages applied to the sample. This assumption was based on mobility data obtained in this study and work conducted by Prunnila et al at room temperature [11]. Mobility data obtained by the author are shown later in figures 5-11 and 5-15.
Two Carrier Types

To extend equations 5.2 and 5.3 to the coexistence regime required consideration of the effects of screening. For example, in Case 1 the electrons are at the front interface while the hole density is increased from zero to some value \( n_h \) at the back interface. Above a certain density the holes screen the 2DEG from the depleting effects of the back gate and \( C_B \) is replaced in equation 5.3 by the capacitance \( C_{eh} \) between the electrons and holes. From this it was assumed that, in this case, any changes in back gate voltage no longer affect the density or conductance of the 2DEG. As the conductance is no longer dependent on both gates the intercept of the \( G_{e,h} \) lines was taken to be the conductance at \( V_{e,h} = 0 \) V, that is, \( G_0 \). Equation 5.3 was then written as

\[
G_{e,h} = g\mu_{e,h} (G_0 - V_{e,h}(C_F + C_{eh}))
\]  

Using the above considerations for the 2DHG in Case 1 with a voltage \( V_h \) applied to it (figure 5-6(a)), it can be seen that above a certain electron density the 2DEG screens the holes from the depleting effects of the front gate. Here \( C_F \) between the 2DHG and the front gate was replaced with \( C_{he} \) in equation 5.4 while \( C_B \) was retained. The electron-hole capacitance was assumed to be purely geometric in nature which set a boundary on its size due to the physical width of the quantum well being 40 nm. Using the equation \( C_{eh,he} = \epsilon_0 \epsilon_{Si}/d_{eh,he} \) where \( \epsilon_0 \) and \( \epsilon_{Si} \) are respectively the permittivities of free space and silicon and \( d_{eh,he} \) is the electron-hole separation. The 'eh' and 'he' denote whether the separation is being measured from the electrons to the holes or vice-a-versa. Obviously these values should be the same for a given set of gate voltages. Additionally, through consideration of the electrostatics of the system, it was expected that for larger asymmetric gate voltages the separation between the carriers would increase. The carrier separations obtained using equation 5.4 would have to be consistent with this picture.

The next section applies equations 5.3 and 5.4 to the experimental data for both Cases 1 and 2. After this section, the inter-layer current is detailed.

5.7 The I-V Characteristics of a 2DEG (2DHG) in the Presence of the Other Carrier Type

The I-V and G-V characteristics are presented here for Cases 1 and 2. After describing the data itself the model described in section 5.6.1 is applied to the results. Both the carrier mobility and electron-hole separations used to fit the G-V results are presented here too. Source-drain voltages at which the inter-layer current is non-zero are considered in section 5.8.

5.7.1 Case 1

For each integer value of the front gate voltage between \( V_F = 6 \) V and \( V_F = 15 \) V back gate voltages between \( V_B = -26 \) V and \( V_B = -50 \) V were applied to the MOSFET. For a constant front and back gate voltage the source-drain voltage was swept from \(-1\) V to 1 V and the
source-drain current measured. Data that shows trends representative of gate voltages around the region of carrier coexistence is used in the following analysis.

The trends in density over the region in and around figure 5-1(iv) are shown in figure 5-8. This figure is used to interpret G-V results in this section. The dashed blue and red lines in figure 5-8 correspond to the lines of $n_e$ and $n_h = 0 \text{ m}^{-2}$ respectively. The ratio of electron to hole densities are also shown across the figure; these ratios were determined from density data, some of which was presented in figure 5-5. This density data was obtained at a source-drain voltage of 10 mV. The greyscale shading is the total current obtained by addition of the electron and hole currents from figure 5-3(a) and (b). The line $AB$ in figure 5-8 is referred to in the text.

![Figure 5-8: Carrier densities for the gate voltages corresponding to Case 1 and figure 5-1(iv). The long-dashed lines are guides to the eye and demarcate the boundaries of the different carrier densities. The green line $AB$ is referred to in the text.](image-url)
Figure 5-9: With the exception of the dashed, dark yellow lines in figures (c) and (d), all data shown here were obtained at \( V_F = 9 \text{ V} \). (a) and (b) Respectively electron and hole current dependence on source-drain voltage. (c) and (d) The differential conductance as a function of source-drain voltage for electrons and holes respectively.

Figure 5-9 shows the I-V and G-V characteristics for both the electrons and holes. Specifically, the electron I-V and G-V data appears in figures 5-9(a) and (c) respectively while the hole I-V and G-V data appears in figures 5-9(b) and (d) respectively. Most of the data presented in figures 5-9(a) to (d) was obtained at \( V_F = 9 \text{ V} \) for the range of back gate voltages shown in the legend. The exception to this is the dashed, dark-yellow line in figures 5-9(b) and (d) that was obtained at \( V_F = 4 \text{ V} \). This line is shown for comparison with the rest of the hole data. The I-V characteristics of the electrons and holes in figures 5-9(a) and (b) are considered first.

At \( V_B = -26 \text{ V} \) in figure 5-9(a) and \( V_B = 4 \text{ V} \) in figure 5-9(b) the trend in I-V is the same as that associated with a single layer of carriers occupying the quantum well. This interpretation is supported by the linear dependence of the electron and hole conductance in figures 5-9(c) and (d) for the same gate voltages [51]. Returning to figure 5-9(a), it can be seen that for positive source-drain voltages the source-drain current \( I_e \) decreases as \( V_B \rightarrow -50 \text{ V} \). The initial decrease in the source-drain current with negative back gate voltage was attributed to the depleting effects of this negative back gate voltage on the electrons. This would reduce their conductance and so lead to the observed drop in source-drain current. As \( V_B \) approaches \(-50 \text{ V} \) the source-drain current ceases to decrease with negative back gate voltage. This occurs as the increasing density of holes close to the BOX/SOI interface is able to screen the electrons near the FOX/SOI interface from the depleting effects of the back gate [11, 126].
A similar dependence of the current through the holes in figure 5-9(b) can be observed. However, because the holes are positively charged, the hole source-drain current \( I_h \) increases as \( V_B \to -50 \text{ V} \) because the hole density increases with back gate voltage. Unlike the electron source-drain current, \( I_e \), it does not saturate with back gate voltage as the 2DHG experiences directly the depleting effects of the back gate voltage as \( V_B \to -26 \text{ V} \). As \( V_B \) approaches \(-26 \text{ V} \), the hole density is reduced and so the current decreases with gate voltage until it becomes zero.

Further interpretation of the data is accomplished by considering figures 5-9(c) and (d); starting with the electron conductance \( G_e \) in figure 5-9(c). The straight line behaviour indicative of a single carrier type existing in the quantum well at \( V_B = -26 \text{ V} \) can be seen to change depending on both the magnitude of the source-drain current and the back gate voltage. Considering first the line at \( V_e = 10 \text{ mV} \) it can be seen that the magnitude of the conductance decreases as \( V_B \to -50 \). As with the electron I-V characteristics in figure 5-9(a), this trend in conductance was attributed to the increasing hole density at the BOX/SOI interface screening the electrons from the depleting effects of the back gate. Additionally, the gradient of the G-V lines increases as \( V_B \to -50 \text{ V} \). To interpret this result, the trends in density along line \( AB \) in figure 5-8 were compared with the trend in gradient along the line \( V_e = 10 \text{ mV} \) in figure 5-9(c). Moving from point A to B in figure 5-8 increases the hole density from zero to values that are eventually greater than the electron density. Following the line \( AB \) in figure 5-9(c) at \( V_e = 10 \text{ mV} \) corresponds to moving from \( V_B = -34 \) to \( V_B = -50 \text{ V} \). From this it was surmised that increasing the hole density increases the gradient of the conductance lines; providing evidence that the conductance characteristics of the 2DEG were affected by the 2DHG. This was thought to occur because as \( n_h \) increases the electrons are no longer gated by the back gate. Instead, they are capacitively coupled to the physically closer 2DHG giving rise to the increase in gradient.

Returning in figure 5-9(c) to \( V_B = -26 \text{ V} \), the effects of applying a positive source-drain voltage to the electrons are now considered. Applying a positive \( V_e \) to the electrons when there is only a 2DEG in the system depletes the electrons in the vicinity of the n-type contact. This leads to the observed decrease in \( G_e \) with increasing source-drain voltage. When \( G_e = 0 \text{ S} \) the electron current in figure 5-9(a) saturates. The linear dependence of \( G_e \) in figure 5-9(c) at \( V_B = -26 \text{ V} \) can also be observed for gate voltages in the range \( V_B = -34 \text{ V} \) to \(-40 \text{ V} \). This is despite the fact that many of these traces initially exhibit a steep gradient in \( G_e \) at \( V_e = 10 \text{ mV} \). A transition from a bilayer system to a single layer one has apparently occurred by applying a positive source-drain voltage to the electrons. This is explained in the following manner. When there is a bilayer system in the quantum well, applying a positive source-drain voltage depletes both the electrons and holes. Depending upon the number of the electrons compared to the number of holes at \( V_e = 10 \text{ mV} \), different effects on \( G_e \) with positive \( V_e \) are observed. Moving along line \( AB \) in figure 5-8 to \( V_B = -40 \text{ V} \) where the hole density is non-zero but smaller than the electron density, both steep and shallow gradients in the \( G_e \) data at \( V_B = -40 \text{ V} \) are observed in figure 5-9(c). As applying a positive \( V_e \) depletes an equal number of electrons and holes, the holes deplete before the electrons and the single layer dependence of \( G_e \) on the
source-drain voltage is returned to.

Substantially different behaviour is observed in $G_e$ on positive $V_e$ when the hole density is greater than the electron density. For a back gate voltages in the range $V_B = -44 \text{ V}$ to $-50 \text{ V}$ $G_e$ goes straight to zero as $V_e$ is increased with no transition to the single-layer dependence observed at less negative back gate voltages. For $V_B = -44 \text{ V}$ to $-50 \text{ V}$, the electrons are depleted before the holes with positive $V_e$. Once the electrons are fully depleted and $G_e = 0 \text{ S}$, $I_e$ in figure 5-9(a) saturates at some non-zero value.

Similar trends are present in the hole data in figure 5-9(d) that were present in the electron data in figure 5-9(c). The main differences arise here from the positive charge of the holes and their proximity to the back gate. The effect of the back gate is evident if, for example, the line at $V_h = 10 \text{ mV}$ is considered. Until the holes are fully depleted at $V_B = -34 \text{ V}$ the hole conductance $G_h$ increases with increasingly negative $V_B$. The effect of the positive charge of the holes is evident in that features present at positive source-drain voltages for the electrons occur at negative source-drain voltages for the holes. A similar transition from a bilayer to a single 2DHG with negative $V_h$ can be observed in the data at large, negative back gate voltages. For example, at $V_B = -50 \text{ V}$ the hole density is greater than the electron density (point B on figure 5-8). Applying a negative $V_h$ to the 2DHG depletes the holes in the vicinity of the p-type contact. Simultaneously, the electrons in the 2DEG are also depleted and, once $n_e = 0 \text{ m}^{-2}$, single carrier behaviour is returned to. For back gate voltages where $n_e > n_h$ the hole conductance goes to zero with negative $V_h$ with no single carrier behaviour observed. This is due to the holes being depleted before the electrons.

**Fitting the Conductance Data**

Both the shallow and steep gradients in figures 5-9(c) and (d) were fitted using the model described in section 5.6.1. Equation 5.3 was used to fit the shallow gradients as these were indicative of a single carrier type occupying the quantum well. The carrier mobility was used as the fitting factor for this fit. Mobilities obtained from the earlier Hall measurements are compared to those values used in equation 5.3 later. Equation 5.4 was used to fit the steep gradients as these were indicative of a a bilayer system within the quantum well. The values of the electron-hole separation used to fit the data are later compared to the nominal thickness of the silicon quantum well.
Figure 5-10: All data shown here is at \( V_F = 9 \) V. (a) and (c) Fitting of the shallow gradients using \( \mu_{e,h} \) as the fitting factor. (b) and (d) Fitting of the steeper gradients from which the electron-hole separation was calculated.

The dotted lines in figures 5-10(a) to (d) are the fits to the data using equations 5.3 and 5.4. Not all of the fitted lines are shown for reasons of clarity. Only one value of the electron or hole mobility was used to fit all of the G-V data in figures 5-10(a) and (b). This was based on the assumption that changing the back gate voltage for a constant front gate voltage had a minimal effect on the carrier mobility. Different mobilities were used to fit the G-V data in the other \( V_F \) figures; note that these figures are not shown here although the mobilities used to fit the data within them will be below. Similarly for the electron-hole separation used to fit the steep gradients in figures 5-10(c) and (d), the separation was assumed to be constant for a constant front gate voltage and back gate voltages in the range where a bilayer occupied the quantum well. One value of the electron-hole separation was used to fit the data for a given \( V_F \). Again, the G-V data at these other front gate voltages do not appear here while the electron-hole separation values used to fit the data within them are shown later.

For the shallow gradients in figures 5-10(a) and (b), the mobility used in equation 5.3 fits the experimental data where only a single carrier gas is present within the quantum well. Another deviation of the experimental data from the fit manifests as the electron or hole conductance approaches zero with the source-drain voltage. This deviation from the fit is most likely due to the low density of electrons or holes at these source-drain voltages being unable to screen the disorder potential at the oxide/SOI interface [51]. The mobilities used to fit the data are shown in figure 5-11(b): the trends in electron and hole mobility with gate voltage are described below. Figures 5-10(c) and (d) have the results of equation 5.4 plotted on them. The predictions by
equation 5.4 appear to fit the $G_e$ data over the region where a bilayer exists in the quantum well. Again, there is a deviation from the fit as the electrons are depleted by the positive source-drain voltage. This is again attributed to the low electron density being unable to screen the disorder potential at the FOX/SOI interface. The fit to the hole data in figure 5-10(d) is only valid for a lower range of the experimental data. For example, at $V_B = -50$ V some linear dependence of $G_h$ on $V_h$ is observed in the region fitted by equation 5.4. As $V_B \to -34$ V the linear dependence of $G_h$ on $V_h$ is lost and the fit to the data provided by equation 5.4 is no longer a good one. Values of the electron-hole separation used to fit the steeper gradients in figures 5-10(c) and (d) are shown in figure 5-11(c).
Figure 5-11: (a) Electron and hole densities over a region of carrier coexistence. (b) Comparison of electron and hole mobilities. The red and black lines correspond to $V_B = -50$ V and $V_B = -40$ V respectively as in (a). (c) Electron-hole separation over the gate voltage range used in this experiment.

The data in figures 5-11(a) and (b) shows carrier density and mobilities as a function of both front and back gate voltages. The back gate voltages used, $V_B = -50$ V and $V_B = -40$, in these figures are ones that correspond to electrons and holes coexisting within the quantum well. The Hall mobilities (crosses) in figure 5-11(b) were calculated from the Hall density data.
that appeared previously in this chapter. The mobilities used to fit the electron and hole conductance appear as vertical crosses for the electrons and circles for the holes. Plotting the data like this allowed the earlier assumption that the carrier mobility remained constant over a range of back gate voltages where a bilayer was present within the quantum well to be checked. Where the holes are concerned the Hall mobilities show no dependence on either \( V_F \) or \( V_B \). The hole mobilities used to fit the \( G_h \) data are consistent with the Hall mobilities to within experimental error. For the electrons it was found that all mobilities showed some dependence on the gate voltages with a decrease in \( \mu_e \) with increasing \( V_F \). This occurs due to the increased effect of the disorder potential on the electrons at the FOX/SOI interface as the electrons are forced closer to that interface with increasing front gate voltage. The dependence of all the \( \mu_e \) on \( V_B \) is qualitatively small in comparison to the dependence on \( V_F \). The fact that most of the Hall mobilities lie within the error bars of the fitted mobilities suggests that the fitted values are accurate compared to those calculated from Hall measurements. The transition from \( n_e > n_h \) to \( n_e < n_h \) appears to have no effect on the carrier mobility. However, the range of densities and mobilities presented here may be too small to observe any effect of the above transition on the carrier mobility.

Figure 5-11(c) shows the electron-hole and hole-electron separations \( d_{eh} \) and \( d_{he} \) respectively. It was expected that these two quantities would be the same as, for a constant front and back gate voltage, it should not matter which layer of carriers the physical separation is measured from. Reasons for this difference are discussed later. Despite this erroneous result, the absolute values of the carrier-carrier separation used in equation 5.4 are less than the nominal thickness (40 nm) of the quantum well. However, the errors in the carrier-carrier separations are significant with respect to their absolute values. Reasons for this large error are also discussed below.

Discussion

The mobilities reported here will now be compared to those values found in the literature. This can only be accomplished for like densities as this ensures the electric field in the quantum well is identical between samples used in the different studies. Similar material systems and crystallographic planes must also be used as the different materials and orientations can demonstrate differing mobilities [10, 11, 48, 123–126]. The study by Prunilla et al. [11] proved ideal as theirs was also conducted at room temperature while the only differences between the samples used in that study and those under analysis in this thesis were the oxide and SOI thicknesses. Table 5.4 compares carrier mobilities from both this study and those determined in [11]. The densities were obtained from data presented in figure 5-11(a).
Table 5.4: Mobilities from this report, both Hall and fitted, and Prunnila et al. No errors were given in their mobility data. Density data over the range in figure 5-11(a) was used in an attempt to obtain full coverage of the system.

<table>
<thead>
<tr>
<th>Carrier Type</th>
<th>Densities ($10^{16}$ m$^{-2}$)</th>
<th>Mobilities ($10^{-2}$m$^{2}$V$^{-1}$s$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrons</td>
<td>1.80 ± 0.01</td>
<td>5.50 ± 0.02, 5.50 ± 0.10, 4.50</td>
</tr>
<tr>
<td>Holes</td>
<td>0.75 ± 0.01</td>
<td>1.00 ± 0.08, 1.00 ± 0.05, 0.50</td>
</tr>
<tr>
<td>Electrons</td>
<td>0.30 ± 0.01</td>
<td>4.75 ± 0.01, 4.80 ± 0.10, 4.75</td>
</tr>
<tr>
<td>Holes</td>
<td>0.13 ± 0.01</td>
<td>1.00 ± 0.06, 1.00 ± 0.05, 0.50</td>
</tr>
</tbody>
</table>

The fact that the mobility is lower in Prunnila et al. is due to their quantum well being narrower (22 nm). This means that although the electric field is the same in both wells the distance from the 2DCG to the oxide interface will be smaller in the narrower quantum well. The carriers will therefore feel the effect of the disorder potential at the oxide interface more strongly than in the wider quantum well used in this thesis. This results in greater scattering of the carriers in the narrower quantum well leading to the observed decrease in carrier mobility.

The separation $d_{eh}$ between the carriers could not be compared directly with any pre-existing data like the mobilities were. Instead the fitted separation was compared to the width of the quantum well and the dependence of $d_{eh}$ on gate voltage analysed for physically consistent results. This trend was expected to result in an increase of $d_{eh}$ with increasingly asymmetric gate voltages. Alternatively, the greater the absolute values of the front and back gate voltages, the greater the electron-hole separation. Although the absolute values of the carrier-carrier separation were physically consistent with the width of the quantum well, the actual predicted values of $d_{eh}$ for a given set of gate voltages are different depending on whether the electron or hole data is used to calculate the separation. It would be expected that $d_{eh}$ was independent of the carrier gas from which it was measured. There are a number of reasons that $d_{eh}$ is different for both carriers and also why the error bars are so large. Firstly, the model is section 5.6.1 used to calculate these values fails to account for the change in carrier density between the source and drain contacts for large source-drain voltages. The capacitance between the electrons and holes will therefore be a function of this distance. Secondly, the large errors arise from the difficulty in fitting the steeper lines as they are not all exactly linear. This is especially true of the hole data as evidenced in figure 5-10 where the steeper hole gradients are more curvy-linear than they are straight. Thirdly the assumption that the back (front) gate is completely screened by the 2DHG (2DEG) is not correct as can be seen by the decrease in $G_0$ with back (front) gate voltage. This would lead to a slight shift in the position of the electrons (holes) within the quantum well, changing the carrier separation.

5.7.2 Case 2

For each integer value of the front gate voltage between $V_F = -6$ V and $V_F = -15$ V back gate voltages between $V_B = 26$ V and $V_B = 50$ V were applied to the MOSFET. For a constant front and back gate voltage the source-drain voltage was swept from $-1$ V to 1 V and the
source-drain current measured. Data that shows trends representative of gate voltages around the region of carrier coexistence is used in the following analysis.

The trends in density over the region in and around figure 5-1(iii) are shown in figure 5-12. This figure is used to interpret G-V results in this section. The dashed blue and red lines in figure 5-8 correspond to the lines of $n_e$ and $n_h = 0 \text{ m}^{-2}$ respectively. The ratio of electron to hole densities are also shown across the figure; these ratios were determined from density data, some of which was presented in figure 5-5. This density data was obtained at a source-drain voltage of 10 mV. The greyscale shading is the total current obtained by addition of the electron and hole currents from figure 5-3(a) and (b). The line $AB$ in figure 5-12 is referred to in the text.

In this Case the electrons were closer to the back interface while the holes were closer to the front. Starting with the electron data in figures 5-13(a) and (c), a greater dependence on the back gate voltage can be observed in both the source-drain current and differential conductance than was observed in the electron data in Case 1. This is due to the fact that the 2DEG was closer to the BOX/SOI interface in this Case and so the electrons directly experienced the depleting effects of the back gate voltage. The results in figures 5-13(a) to (d) are interpreted in a similar manner to figures 5-9(a) to (d) in Case 1. Considering the electron data in figure 5-13(c) for $V_B = 50 \text{ V}$ to $42 \text{ V}$ it can be observed that both steep and shallow gradients in $G_e$ are present. This arises for similar reasons as discussed in Case 1. When $n_e > n_h$ (figure 5-12), the holes deplete before the electrons with positive $V_e$ and the quantum well hosts a 2DEG only. For gate voltages where $n_e < n_h$ the electrons are depleted before the holes and no single carrier behaviour is observed in figure 5-13(c). The holes, now closer to the FOX/SOI interface, show a screening of $G_h$ with increasingly positive back gate voltage as the electron density increases and starts to screen the holes from the depleting effects of the back gate. For the hole conductance data in figure 5-13(d) a similar dependence of $G_h$ on $V_h$ and the ratio of the electron and hole densities is observed. For gate voltages where $n_h > n_e$ the steep gradient present at low $V_h$ is turned into a shallow gradient indicative of a single 2DHG occupying the quantum well. Conversely, for gate voltages where $n_h < n_e$, only the steep gradient associated with an electron-hole bilayer is observed. In this instance, $G_h$ goes straight to zero with negative $V_h$. 84
Figure 5-12: Carrier densities for the gate voltages corresponding to Case 1 and figure 5-1(iii). The long-dashed lines are guides to the eye and demarcate the boundaries of the different carrier densities. The green line AB is referred to in the text.

Figure 5-13: Unless otherwise stated, all data shown here was obtained at $V_F = -10$ V. This gate voltage produced a similar carrier density to that used for Case 1. (a) and (b) Electron and hole current dependence on source-drain voltage respectively. (c) and (d) The differential conductance as a function of source-drain voltage for electrons and holes respectively. The line at $V_B = 26$ V in (d) has been offset by $-0.87 \mu S$. 

Legend:
- $V_e$ (V)
- 50
- 48
- 46
- 44
- 42
- 40
- 38
- 36
- 34
- 26
Fitting the Conductance Data

The results of using equations 5.3 and 5.4 to fit the data in figures 5-13(c) and (d) are shown in figure 5-14. The mobilities and electron-hole separations used to fit the data appear to give good agreement with most of the experimental data over the single carrier or bilayer regimes. The hole conductance data in figure 5-14(d) demonstrates a deviation from the straight lines observed in previous data for both the single and coexisting carrier systems. Where the single carrier behaviour is concerned this could be related to the disorder potential at the FOX/SOI interface. As the hole density is decreased by $V_h$, the 2DHG cannot effectively screen the disorder potential and so the carrier mobility decreases due to the extra scattering of the particles.

![Graph showing conductance data fitting](image)

Figure 5-14: Unless otherwise stated, all data shown here is at $V_F = -10$ V. (a) and (c) Fitting of the shallow gradients using $\mu_{e,h}$ as the fitting factor. The legend used in (a) should also be used for figures (c) to (d). (b) and (d) Fitting of the steeper gradients from which the electron-hole separation is calculated.

The carrier mobilities and electron-hole separations used to fit the data are plotted as a function of front gate voltage in figures 5-15(b) and (c) respectively. In a similar manner to that in Case 1, the mobility was assumed to remain constant for the values of $V_B$ used when applying a constant front gate voltage. Additionally, the electron-hole separation was assumed to remain constant for all $V_B$ when applying a constant front gate voltage. Figure 5-15(b) shows that the majority of the Hall mobilities lie within the error bars of the mobilities predicted by equation 5.3.
Figure 5-15: (a) Electron and hole densities over a region of carrier coexistence. (b) Comparison of electron and hole mobilities. The red and black lines correspond to $V_B = 50 \text{ V}$ and $V_B = 40 \text{ V}$ respectively as in (a). (c) Electron-hole separation.

Discussion

It difficult to determine whether the $\mu_h$ at $V_F = -8 \text{ V}$ and $-7 \text{ V}$ are accurate as compared to Hall mobilities as no Hall data existed for the 2DHG at these gate voltages. This was due to the
hole current being too small to measure at the $V_h = 10 \text{ mV}$ used for Hall measurements. The
electron mobilities predicted by equation 5.3 are somewhat smaller than their Hall counterparts.
Qualitatively, the trend observed in the predicted mobilities as a function of $V_F$ is similar to
that observed in the Hall mobility as a function of $V_F$. Like the Hall mobilities, the fitted
mobilities are initially low at large negative $V_F$ followed by a rise over a certain voltage range
before plateauing for all further $V_F$. Comparing figures 5-15(a) and (b) it can be seen where
$n_e = n_h$ a plateau has already occurred in the corresponding Hall mobility data. From figure
5-15(a), as $n_h \to 0 \text{ m}^{-2}$ the Hall mobilities continue with their plateau-trend. Where the fitted
mobilities are concerned the plateau occurs when $n_e > n_h$ for both back gate voltage values. It
is possible that the fitted mobilities plateau at this point due to the fact that, on figure 5-3(d),
$n_h \to 0 \text{ m}^{-2}$ as $V_F \to 0 \text{ V}$. These mobilities are compared to those in the work of Prunilla et al

<table>
<thead>
<tr>
<th>Carrier Type</th>
<th>Densities ($10^{16} \text{ m}^{-2}$)</th>
<th>Mobilities ($10^{-2} \text{m}^2\text{V}^{-1}\text{s}^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hall</td>
<td>Fitted</td>
</tr>
<tr>
<td>Electrons</td>
<td>0.13 ± 0.01</td>
<td>5.30 ± 0.01</td>
</tr>
<tr>
<td>Holes</td>
<td>0.75 ± 0.01</td>
<td>0.75 ± 0.04</td>
</tr>
<tr>
<td>Electrons</td>
<td>1.125 ± 0.01</td>
<td>5.40 ± 0.01</td>
</tr>
<tr>
<td>Holes</td>
<td>2.00 ± 0.05</td>
<td>0.75 ± 0.05</td>
</tr>
</tbody>
</table>

Table 5.5: Mobilities from this report, both Hall and fitted, and Prunilla et al. No errors
were given in their mobility data. Density values were selected over the full range of data were
possible from figure 5-15(a).

Table 5.5 shows that he Hall mobilities demonstrate the greatest difference when compared
with data from Prunilla et al. [11]. Without errors for Prunilla’s data it is not possible
to determine whether the electron Hall mobilities are larger than might be expected when
compared to a narrower quantum well.

Values of the electron-hole separation in figure 5-15(c) show similar results to those of figure
5-10(c) where again a discrepancy between using the electron or hole data to determine the
carrier-carrier separation quantity is observed. Here, the holes at the front produce a separation
that increases with more negative front gate voltages, as would be expected by considering the
electrostatics of the system. However, it appears that using the electron data to determine
d_{eh}, without error bars, produces the unphysical result that a greater gate voltage reduces the
carrier separation. As previously stated the reasons for the large errors are most likely due to a
combination of the fact that the electron-hole capacitance is a function of the distance between
the source and drain contacts for large source-drain voltages, the difficulty in accurately fitting
the steeper lines in the G-V characteristics and the incorrect assumption that the far gate is
completely screened by the other carrier type.
5.8 The Inter-Layer Current

For certain source-drain voltages a current was observed passing from the electrons to the holes or vice-a-versa depending on the setup in figure 5-6 used. This current was labeled $I_{eh}$ or $I_{he}$ where the first letter denotes which carrier the source-drain voltage was applied to while the second letter denotes through which carrier type the current flowed. A qualitative model is detailed in this section for the behaviour of this current.

5.8.1 Modeling the Inter-Layer Current

To model the interlayer current some observations about its nature were first considered. Figures 5-17 and 5-19 show that the interlayer current was non-zero for voltages of the same sign as the charge carrier to which the source-drain voltage was being applied. For example, in Case 1 a voltage $V_e$ was applied to the 2DEG via an n-type contact. When $V_e \geq 0$ V the interlayer current was zero or below $10^{-11}$ A on figures 5-17(c) and (e). For $V_e \leq 0$ V the interlayer current became non-zero. For a source-drain voltage applied to a 2DHG via a p-type contact the interlayer current was non-zero for positive $V_h$. When negative (positive) voltages are applied to an n-type (p-type) contact the electron (hole) density in the local region around that contact increases [51]. From this arose the idea that the current could be passing from the n-type (p-type) contact to the 2DHG (2DEG). If this were the case then the interlayer current would be non-zero even for gate voltages where no 2DEG (2DHG) was present. Additionally the inter-layer current would display p-n junction-like characteristics due to the built-in potential barrier that existed between the n-type (p-type) region and the 2DHG (2DEG). Once a current was flowing through the 2DHG (2DEG) the I-V characteristics were predicted to be quadratic in nature owing to the fact that, despite the presence of a p-n like-junction, a source-drain voltage was being applied to the 2DHG (2DEG). Schematic diagrams of the different currents and resistances for both electron and hole systems are shown figure 5-16. It was assumed that there were only three resistances that affect the interlayer current. These were the resistances of the 2DEG ($R_{2DEG}$), 2DHG ($R_{2DHG}$) and the current channel that existed between the electrons and holes ($R_{pn}$).

![Figure 5-16: (a) and (b) Are respectively schematic diagrams to aid in understanding the resistances that affect the inter-layer current for the electrons and holes.](image)

Depending on the relative sizes of $R_{2DEG}$, $R_{2DHG}$ and $R_{pn}$ would determine whether quadratic
or exponential behaviour of the interlayer current was observed. The resistances of the 2DEG and 2DHG were dependent primarily on the carrier densities within their respective layers.

$I_{eh}$ was plotted on both log-lin and log-log plots. The former would reveal any diode-like behaviour while the latter any quadratic dependence on the source-drain voltage. The interlayer currents $I_{eh}$ and $I_{he}$ are considered separately for Cases 1 and 2 below.

### 5.8.2 Case 1

Considering first the electrons in figures 5-17(c) and (e) it can be seen that at $V_e = 0$ V, $I_{eh}$ is negligible. From figures 5-8 and 5-17(c) when $V_B = -30$ V, $V_F = 9$ V and $V_e = 10$ mV it was found that $n_e > 0$ m$^{-2}$ while $n_h \approx 0$ m$^{-2}$. Figure 5-17(c) shows that, under the same gate voltages, a source drain voltage of $\approx -0.75$ V is required to generate even a small inter-layer current. This magnitude of $V_e$ is required as the density of holes in the local area around the n-type contact must be first increased in order to pass a current through the region. This reduced the potential barrier between the two carrier types allowing for conduction to occur. When $V_B \geq -34$ V a substantial density of both electrons and hole existed in the quantum well and the source-drain voltage required to observe an interlayer current dropped substantially to $\approx -0.125$ V. Increasing $n_e$ by raising $V_F$ from 9 V to 15 V appears to have a negligible impact on magnitude of $I_{eh}$ for the following reason. The holes at the BOX/SOI interface are screened from the depleting effects of the front gate voltage. This means any current flowing through the 2DHG will also be screened from the front gate and so will not demonstrate any dependence on that gate voltage.
Figure 5-17: Legend 1 (solid lines) corresponds to changing $V_B$ for the constant $V_F$ shown in the above figures. Legend 2 (dotted lines) corresponds to the data in figures (d) and (f) at a constant $V_B = -50$ V for the different $V_F$ shown in Legend 2. (a) and (b) Expanded voltage ranges of figures 5-9(c) and (d) demonstrating the effects of the interlayer current on the differential conductance. (a) and (b) Show the effects of the inter-layer current on the differential conductance of both carriers. (c) and (d) Inter-layer current at $V_F = 9$ V. (e) and (f) Inter-layer current at $V_F = 15$ V.

Considering the hole data in figures 5-17(d) and (f) where the holes were at the BOX/SOI interface with the inter-layer current flowing from the p-type contact through the 2DEG. it can be seen that there is virtually no dependence of the interlayer current $I_{he}$ on $V_B$. This occurred because the 2DHG was at the back interface while the electrons through which $I_{he}$ traveled were at the front interface. As the electrons were screened from the effects of the back gate the interlayer current remained unaffected by any change in back gate voltage. There was a similar lack of dependence on front gate voltage between $V_F = 9$ V and $V_F = 15$ V (figures 5-17(d) and (f) respectively). Reducing the front gate voltage to $V_F = 4$ V up to 6 V where the electron density was small and applying a constant $V_B = -50$ V shows that there is a dependence of $I_{he}$ on $V_F$ for large $V_h$ (dotted lines on figures 5-17(d) and (f)). It was surmised that at $V_F = 4$ V the source-drain voltage was too low for all applied $V_h$ to overcome the potential barrier and instigate a non-zero $I_{he}$. It would be expected that the linear trace at $V_F = 6$ V and $V_B = -50$
V in figure 5-17(d) would develop with increasing front gate voltage to that observed at \( V_F = 9 \) V and \( V_B = -50 \) V. In doing so the linear relationship displayed at \( V_F = 4 \) V undergoes a dramatic change, not only increasing in magnitude but also changing in its dependence on the applied source-drain voltage. The linear dependence of \( I_{he} \) at low electron density suggested an exponential dependence of \( I_{he} \) on \( V_h \). This was thought to be caused by the p-n like junction described earlier in this section. As \( V_F \) is increased towards 9 V the trend changes into one that contains both the supposed exponential dependence at low \( V_h \) and some other functional dependence at higher source-drain voltages. At these higher electron densities it would be expected that a quadratic dependence of \( I_{he} \) on \( V_h \) would exist as the inter-layer current flows through a 2D carrier gas. This was checked for by plotting the interlayer current on a log-log plot. The results of plotting the interlayer current on both lin-log and log-log graphs is shown in figure 5-18 for both electrons and holes.

![Graphs showing exponential and quadratic dependencies](image)

Figure 5-18: Legend 1 (solid lines) corresponds to changing \( V_B \) for the constant \( V_F \) shown in the above figures. Legend 2 (dotted lines) corresponds to the data in figures (d) and (f) at a constant \( V_B = -50 \) V for the different \( V_F \) shown in Legend 2. The long dashed green lines are those used to determine the gradients of the data. (a) and (c) Certain regions of these graphs demonstrate an exponential dependence of \( I_{ch,he} \) on \( V_{ch,h} \). (b) Although the quadratic dependence appears minimal for higher \( n_{th} \), it may return at higher \( V_c \). (d) The trend here also deviates from the quadratic dependence before appearing to tend back towards it at higher \( V_h \).

In fitting the lines on figure 5-18 at least 40 data points were used per line, corresponding to a source-drain voltage of 0.14 V. For the exponential gradients (figures 5-18(a) and (c)) the diode equation was used [51]

\[
I_{ch,he} = I_s(e^{\pm \frac{V_{ch,h}}{kT}} - 1) \tag{5.5}
\]
where $I_s$ is the saturation current, $e$ the electronic charge, $k_B$ Boltzmann’s constant, $\eta$ is the ideality factor and $T$ the absolute temperature of the p-n junction. As the diode existed between an n-type (p-type) contact and a 2D carrier system it was assumed that it was not an ideal diode as per the Ideal Shockley Diode equation where $\eta = 1$. The gradient of the exponential line is given by $(1/\eta) \times (e/k_B \times T)$ which allowed estimates of $\eta$ assuming p-n junction temperature of 300 K. An increase in this value of 20 K was assumed to account for any heating effects [51]. The p-n junction ideality factors and gradients used to calculate them are shown in table 5.6. The values are larger than the ideal diode value of 2 because this was not an actual diode but instead diode-like.

<table>
<thead>
<tr>
<th>Figure</th>
<th>Gradient</th>
<th>$\eta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-18(a)</td>
<td>7.77 ± 0.02</td>
<td>4.85 ± 0.15</td>
</tr>
<tr>
<td>5-18(b)</td>
<td>2.21 ± 0.05</td>
<td>-</td>
</tr>
<tr>
<td>5-18(c)</td>
<td>8.37 ± 0.04</td>
<td>4.45 ± 0.15</td>
</tr>
<tr>
<td>5-18(d)</td>
<td>3.32 ± 0.29</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 5.6: Gradients from lines fitted to data in figure 5-18. $\eta$ values of the p-n junction are given for the exponential gradients only.

The gradients from figures 5-18(b) and (d) are also shown in table 5.6. The electron data in figure 5-18(b) shows a gradient that is close to 2 as would be expected of a quadratic relationship. Although the value returned for the holes is close to 2 the error associated with the value is large due to it being obtained in the low current region of the graph at the periphery of the current that the Keithley SMU could accurately measure. It is noted that the gradients of both figures 5-18(b) and (d) appear to tend towards a value of 2 as the applied source-drain voltage approaches 1 V suggesting quadratic behaviour at higher carrier densities and source drain voltages. However, because there were few data points at this extreme source-drain voltage it is difficult to definitively quantify whether this trend will continue or change once $V_{c,h}$ exceeds 1 V.
5.8.3 Case 2

Here the electrons were at the back interface while the holes were at the front. The data in figures 5-19(a) to (d) is shown at $V_F = -10$ V as this gives a similar electron and hole densities to the data at $V_F = 9$ V in figures 5-18(a) to (d).

![Legend: $V_S (V)$
- 50
- 48
- 46
- 44
- 42
- 40
- 38
- 36
- 34
- 32
- 30
- 28
- 26](image)

![Figure 5-19: (a) and (b) The differential conductance of the electrons and holes over the $V_{eh,h}$ range where $I_{eh,he}$ is non-zero. (c) $I_{eh}$ demonstrates a low dependence on $V_B$ while in (d) $I_{he}$ is dependent on $V_B$ until large $n_e$ is reached. (e) and (f) Aside from changes in the absolute values of $I_{eh,he}$, these are qualitatively similar to (c) and (d).](image)

The screening previously observed in $I_{he}$ is now observed in $I_{eh}$ as the interlayer current is passing from the n-type contact through the holes at the front interface (figures 5-19(c) and (e)). The 2DHG and the interlayer current traveling through it are both screened from the effects of the back gate when there is a 2DEG at the back interface. Estimates of both exponential and quadratic dependencies of $I_{eh,he}$ on the source-drain voltage are presented in table 5.7. The lines used to obtain the gradients and, where relevant, the ideality factors of the p-n junction
are shown in figure 5-20.

Some of the data demonstrates both exponential and quadratic behaviour at a single back gate voltage. An example of this is the $I_{he}$ data at $V_B = 30$ V in figure 5-20(d).

<table>
<thead>
<tr>
<th>Figure</th>
<th>Gradient $\eta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-20(a)</td>
<td>$7.34 \pm 0.03$ 5.10 $\pm 0.20$</td>
</tr>
<tr>
<td>5-20(b)</td>
<td>$3.05 \pm 0.50$ -</td>
</tr>
<tr>
<td>5-20(c)</td>
<td>$7.01 \pm 0.01$ 5.35 $\pm 0.15$</td>
</tr>
<tr>
<td>5-20(d)</td>
<td>$2.50 \pm 0.27$ -</td>
</tr>
</tbody>
</table>

Table 5.7: Gradients from lines fitted to data in figure 5-20. Ideality values of the p-n junction are given for the exponential gradients only.

As with Case 1, the ideality factors predicted for the exponential lines are larger than those for an ideal diode. Again, this was most likely due to the diode being non-ideal. The fact the values in table 5.7 are rather different to those in table 5.6 is most likely due to the larger error in determining the gradients of the data used to calculate these $\eta$ values. The quadratic fits both produce large relative errors as they were obtained close to the lower range of the measuring range of the Keithley SMU. The gradient in figures 5-20(b) and (d) does appear to tend towards 2 but more current data at higher $V_{c,h}$ is required in order to substantiate whether
this trend will continue.

5.9 Summary of the Chapter and Closing Comments

The data presented here showed for the first time that the I-V characteristics of a 2DEG (2DHG) in the presence of the other carrier type are strongly affected by the presence of the other carrier type. By applying a source-drain voltage to the relevant contact it was shown that the carrier densities could be controlled, changing the system inhabiting the quantum well from that of a bilayer to a single layer. The resulting single carrier I-V characteristics were modeled using equation 5.3. Where Case 1 was concerned the fitted electron mobilities agreed to within their error bars with Hall data. These values were found to agree with results obtained by Prunilla et al. [11]. Mobilities found for Case 2 were lower than the Hall mobilities found over the same gate voltage range. This was most likely due to some error in obtaining the Hall densities and mobilities over this gate voltage range. It is recommended for future work that more Hall data is obtained, not just for the region covered by Case 2 but over a greater range of gate voltages. This would allow for further analysis of the fitted mobilities and minimise the possibility of erroneous data being used.

The determination of the electron-hole separation produced results that, although generally consistent with the 40 nm wide quantum well, contained large errors. It was thought that these errors occurred for the following reasons. To begin, the assumption that the electron-hole capacitance was constant along the line connecting the source-drain contacts was incorrect for large source drain voltages where the carrier density becomes a function of this distance. The model described in this chapter therefore needs to be amended to account for this change of density with distance between the source-drain contacts. A more reliable method must be used when attempting to fit straight lines to these steeper parts of the G-V data especially where the data presents a curvy-linear dependence on the source-drain voltage rather than a linear dependence. The final assertion that back (front) gate was completely screened by the 2DHG (2DEG) was also incorrect as can be seen by the decrease in $G_0$ with back (front) gate voltage. Determining the amount of screening performed by a given density of carriers could potentially enhance the accuracy of the carrier separation calculation. This could be achieved by utilising Thomas-Fermi screening theory [70] to estimate the screening ability of the carriers.

As detailed above, for certain source-drain voltages an interlayer current was observed passing through the carrier type to which the source-drain voltage was being applied. This was thought to be due to the potential barrier between the n-type (p-type) contact and the 2DHG (2DEG) being overcome. The experimental data for $I_{ch,he}$ was analysed in such a way so as to determine whether any exponential or quadratic dependencies of the observed current on the source-drain voltage existed. It was determined that a p-n-like junction existed between the n- or p-type contact and the 2DHG or 2DEH respectively. Further insight into the interlayer current in future work could investigate the temperature and gate voltage dependence of the saturation current $I_s$ and thermal voltage $V_T = k_B T/e$. This would provide information about the potential barrier between the doped contact and the carrier type through which the
interlayer current flows.
Chapter 6

Control of the $g^*m^*$ of a 2DHG on the Si (001) Plane

6.1 Introduction

In this chapter the effective $g$-factor $g^*$ is shown to be controllable on the Si (001) plane using the gates of a Si-MOSFET. The methods used to determine $g^*m^*$ are discussed in detail and the assumptions underlying these methods explained. Additionally, magnetoresistance data obtained by Niida Yoshitaka in his thesis [127] is utilised in order to demonstrate the control of $g^*m^*$ with the MOSFET gates.

The data used to calculate $g^*$ was obtained at the CNRS in Grenoble as described in Chapter 4.

6.2 Background

As described in Chapter 2, even without any external magnetic field, an electric field applied perpendicular to a 2DHG will give rise to an effective magnetic field for holes moving through the electric field. This is the Rashba effect and has been utilised to investigate the spin-orbit (SO) coupling of charge carriers in a range of semiconducting materials. [13–15, 18–21, 33, 34, 38, 71].

In some semiconducting systems, control of the effective $g$-factor ($g^*$) with out-of-plane electric field applied via the transistor’s gates has been demonstrated and used as a means to investigate the SO interaction [19–21]. In silicon based systems the holes have received attention over the electrons the latter possess an effective $g$-factor close to their 'bare' value of $g^*$ 2.02 [71]. Additionally, in silicon quantum wells with SiO$_2$ oxide interfaces, the dielectric constant of the oxide allows for large electric fields to be applied to the 2D hole system in the quantum well. This enables the effective $g$-factor to be varied over a wide range of gate voltages which may result in increased control of the carrier spin. Although this has been demonstrated by Roddaro et al. [92] and Ares et al., these reports utilised Si/SiGe based devices. Control of $g^*$ on the
(001) plane of silicon in an Si-MOSFET has yet to be demonstrated.

In this work the control of $g^*m^*$ on the Si (001) plane of a Si-MOSFET is demonstrated using both data obtained by the author and results reported by our collaborator, Niida Yoshitaka, in his thesis [127]. The reasons for using data from that work are described in the next section.

6.2.1 Our Collaborator’s Data

In experiments performed by the author on the 2DHG both out-of-plane and in-plane magnetic fields were applied independently to the sample to measure the hole density and in-plane magnetoresistance respectively. This allowed for the extraction of a value of $g^*m^*$. In work by our collaborator [127], both an in-plane and out-of-plane magnetic field were applied simultaneously to a Si-MOSFET of a similar cross-sectional structure to those described elsewhere in this thesis. The perpendicular component was kept constant while the in-plane component was increased. In this manner, the cyclotron splitting remained constant while the Zeeman splitting increased with the in-plane field. This sweeping of the Zeeman splitting with respect to the cyclotron splitting lead to changes in the observed filling factors $\nu$. Additionally, the values of $\nu$ were, for constant in- and out-of-plane magnetic fields, found to vary with carrier density and $\delta n$ [127]. Applying the value of $g^*m^*$ determined by the author to Niida’s data allowed for the dependence of $g^*m^*$ on $n$ and $\delta n$ to be demonstrated. The rest of this chapter details first how $g^*m^*$ was determined followed by a description of the experiments performed in [127]. Additionally, the assumptions underlying the application of $g^*m^*$ to the data obtained by Niida are explained.

6.3 Experimental Determination of $g^*$

Here the samples used in experiments are then introduced and followed by an explanation of the extraction of carrier densities and filling factors. In-plane magneto-resistance measurements allowed for the extraction of the magnetic field required to spin polarise a given density of holes. The data obtained from this is then used to calculate $g^*m^*$.

6.3.1 The Samples

The two samples used for experiments were cut from the same wafer shown in figure 3-1. Both possessed front and buried oxide thicknesses of 81 nm and 380 nm respectively while the SOI layer was 40 nm wide. Only their geometric factors $W/L$ were different - Sample A had $W/L = 8/10$ while Sample B had $W/L = 10/10$. The units for both widths and lengths is $\mu$m. These are summarised in table 6.1.

<table>
<thead>
<tr>
<th>Sample</th>
<th>W/L</th>
<th>$d_{SOI}$ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>8/10</td>
<td>40</td>
</tr>
<tr>
<td>B</td>
<td>10/10</td>
<td>40</td>
</tr>
</tbody>
</table>

Table 6.1: Aspect ratios $W/L$ and quantum well thicknesses of Samples A and B.
An oscillating voltage of 10 mV and frequency 13.74 Hz was applied to a p-type contact and the source-drain contact measured as a function of front and back gate voltages and \( V_{xx} \) and \( V_{xy} \). As will be described later, \( V_{xy} \) was used to check that the sample was either perpendicular or parallel to the magnetic field. The experimental setup for out-of and in-plane magnetoresistance measurements was described in Chapters 2 and 4. At room temperature the samples appeared to function correctly with no leaks or short-circuits present. Upon cooling to 1.4 K it became apparent that the back oxide of Sample A leaked current to the SOI at voltages other than \( V_B = 0 \) V. As a result, data was obtained for a range of front gate voltages at \( V_B = 0 \) V for Sample A. As will be shown later, the gates of Sample B were shortcircuited such that any voltage applied to one gate was also applied to the other.

### 6.3.2 Out-Of-Plane Magnetic Field Measurements

To ensure the magnetic field was indeed perpendicular to the sample, \( V_{xy} \) was measured while the device was rotated within the field. When a maximum in \( V_{xy} \) was found, the sample was judged to be at right angles to the field. For a constant set of front and back gate voltages the magnetic field was swept from 0 T to 28 T with the field applied perpendicular to the 2DHG. Figure 6-1 shows experimental data for Sample A while 6-2 shows results for B. Sample A demonstrated that something was wrong with the \( V_{xy} \) measurement as \( \rho_{xx} \) and \( \rho_{xy} \) were similar in their dependence on the magnetic field. This result was deemed to be incorrect and so \( \rho_{xy} \) for Sample A was discarded. Carrier densities could still be estimated for Sample A as the minima in \( \rho_{xx} \) showed the magnetic field range where the plateaus in \( \rho_{xy} \) occurred. It is unknown exactly why \( \rho_{xx} \) and \( \rho_{xy} \) were similar although it was suggested that there was a short-circuit between the \( V_{xx} \) and \( V_{xy} \) probes.

![Figure 6-1: Magneto-resistance data from Sample A. The similarity between \( \rho_{xx} \) and \( \rho_{xy} \) led to suspicions that \( V_{xy} \) had been measured incorrectly. The smaller figure shows the full extent of \( \rho_{xx} \) and \( \rho_{xy} \) at \( V_F = -2.5 \) V.](image)

The \( \rho_{xx} \) and \( \rho_{xy} \) from Sample B show trends that are associated with the quantum Hall
effect as described in Chapter 2. At zero magnetic field the resistivity increases as the front gate voltage tends to 0 V. This occurs due to the decrease in hole density as $V_F \to 0$ V. As $n_h$ decreases the 2DHG cannot screen the effect of the disorder potential generated by the FOX/SOI interface as well as it could at higher densities leading to a decrease in the carrier mobility [128]. For front gate voltages where the density was large, $\rho_{xy}$ demonstrated plateaus as was expected. However at low front gate voltages ($V_F = -1$ and $-1.5$ V) and low densities, these plateaus disappear as the hole screening wavefunction increases in response to the increasing magnetic field [71]. Also apparent at these low densities is noise caused by the lower number of conductance channels available to the carriers. There is some deviation from a flat plateau in the $V_F = -2$ V data in figure 6-2(b) and additionally $\rho_{xx} \neq 0$ over some magnetic field range in figure 6-2(a). This deviation from a flat plateau may have been caused by incomplete screening by the holes of the disorder potential at the Si/SiO$_2$ interface. Thus a decrease in the hole mobility would be expected and a resulting increase in the $\rho_{xx}$ data observed. This scattering would lift the insulating state that the system attains at higher densities [129].

![Sample B](image)

Figure 6-2: Magneto-resistance data from Sample B. (a) $\rho_{xx}$ demonstrating Shubnikov-de-Haas oscillations. The smaller figure contains data for $\rho_{xx}$ at $V_F = -1$ and $-1.5$ V. (b) Quantum Hall plateaus in $\rho_{xy}$. The smaller figures contain $\rho_{xy}$ data at $V_F = -1$ and $-1.5$ V.
The densities determined in the following sections will later be used in conjunction with the in-plane magnetoresistance data to determine what in-plane field led to a fully spin polarised 2DHG for a given hole density.

**Finding The Filling Factors**

Identifying minima in $\rho_{xx}$ where the filling factor $\nu$ took integer values was achieved by comparing the plateaus in $\rho_{xy}$ with minima in $\rho_{xx}$. The filling factor itself was determined by dividing the $\rho_{xy}$ where the plateaus occurred by $h/e^2$ as described in Chapter 2. The values of magnetic field $B$ at a given $\nu$ were plotted as a function of $V_F$, shown as crosses in figure 6-3. These experimental values were checked using equations 6.1 to 6.2 in order to determine whether the experimental values of $\nu$ were accurate. Both sets of $\nu$ are plotted in in figure 6-3; the equations are shown below

$$n_h e = C_F (V_F - V_F^{Th}) + C_B (V_B - V_B^{Th}), \quad n_h = \nu \frac{eB}{h} \quad (6.1)$$

where $B$ is the magnetic field, $\nu$ is the filling factor and the other constants retain their usual meanings. While $C_F$ was determined using the relation

$$C_F = \frac{e\nu}{h} \frac{\partial V_F}{\partial B} \quad (6.2)$$

$C_B$ could not be found from the data as only $V_B = 0$ V was applied to the back gate. Thus calculating the dotted $\nu$ in figure 6-3 using the extra $C_B V_B^{Th}$ term was counted as part of the front gate threshold voltage $V_F^{Th}$

$$B = \frac{h}{e^2 \nu} (C_F V_F - V_F^{Th}) \quad (6.3)$$

The values of $C_F$ and $V_F^{Th}$ used to fit the data are shown in table 6.2. Additionally, the capacitance of the FOX ($C_{FOX}$) was calculated using its nominal thicknesses and appears in table 6.2 for comparison with the experimentally determined value. The thicknesses used to calculate $C_{FOX}$ was $d_{FOX} = 81 \pm 1$.

<table>
<thead>
<tr>
<th>Sample</th>
<th>$C_{FOX}$ ($\mu$Fm$^2$)</th>
<th>$C_F$ ($\mu$Fm$^2$)</th>
<th>$V_F^{Th}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>426 ± 5</td>
<td>412 ± 5</td>
<td>-1.27 ± 0.30</td>
</tr>
<tr>
<td>B</td>
<td>426 ± 5</td>
<td>345 ± 9</td>
<td>0.00 ± 0.36</td>
</tr>
</tbody>
</table>

Table 6.2: $C_F$ and $V_F^{Th}$ for Samples A and B.

Sample B possesses a noticeably different value from both the nominal capacitance $C_{FOX}$ and the capacitance calculated using data from Sample A. The fact that the capacitances were not similar suggested the gates of at least one of the samples was not working correctly. Under investigation it became apparent that the gates of Sample B were short-circuited. Thus, any voltage applied to the front gate was simultaneously applied to the back gate. Comparing the carrier densities of both samples also showed a discrepancy that could be attributed to this problem. The capacitance $C_F$ calculated for Sample B is considerably smaller than the nominal
value which is most likely due to the 2DHG not being at the exact location of the FOX/SOI interface. This would make the experimental value larger than the nominal value.

![Graph](attachment:image.png)

Figure 6-3: The data points are $\nu$ from figures 6-1 and 6-2 while the dotted lines were calculated using equation 6.3. The discrepancy between the two samples was attributed to a short-circuit between the gates of Sample B.

The values of $V_F^{\text{Th}}$ differ significantly between the samples. Again, this was most likely due to the shortcircuit between the front and back gates of Sample B altering the threshold voltage for which no holes were present in the silicon quantum well.

Densities and Mobilities From Shubnikov-de-Haas Oscillations

Densities were calculated using equation 6.1 and the magnetic field values obtained from figures 6-1 and 6-2. For a given $V_F$ the densities were found to be the same irrespective of the $\nu$ value providing further evidence that the values of $\nu$ obtained from 6-1 and 6-2 were consistent. The error bars were calculated using the error in $C_F$ for each sample. These errors were not enough to account for the difference in $n_h$ for similar $V_F$ for the two devices. The gradients are not similar either showing again that the capacitances are indeed different between the two datasets. This added weight to the idea that the gates of Sample B were short-circuited together as the
total density of holes within that Sample's quantum well was greater than the density in Sample A for the same gate voltages. The mobilities, calculated from $1/en\rho_{xx}$ using $\rho_{xx}$ at $B = 0$ T, are displayed in figure 6-5. Although a similar trend in evidenced by the mobility data for both samples, the absolute values are markedly different. Again, this was thought to be due to the short-circuited gates of Sample B producing a 2DHG at the BOX/SOI interface.

![Figure 6-4: For each sample it was found that for a given $V_F$ the densities were similar for the same $\nu$.](image)

![Figure 6-5: Although the trends in mobility are qualitatively similar between the samples, the absolute values are noticeably different.](image)

6.3.3 In-Plane Magneto-Resistance

The samples were rotated through 90° and subjected to similar gate voltages as were used in the transverse measurements. To ensure correct alignment between the sample and magnetic field $V_{xy}$ was measured whilst the sample was rotated within the field. When $V_{xy}$ was at a minimum the sample was taken to be aligned with the magnetic field. Again, only $V_B = 0$ V was used due to the leaky buried oxide. General trends of $\log(\rho_{xx})$ as a function of the in-plane magnetic field in figures 6-6 and 6-7 include a marked increase in the resistivity of the 2DHG as the magnetic field is increased. For lower densities this increase is especially large, hence the term giant magnetoresistance being used to describe it [12]. At higher densities, after the rise of $\rho_{xx}$,
a shoulder in $\rho_{xx}$ is passed and the resistivity plateaus. This shoulder is interpreted to occur when the holes are fully spin polarised; the greater the hole density, the greater the magnetic field required to spin polarise them [12, 130]. This giant magnetoresistance is caused by the screening wavelength of the holes increasing in response to the increasing magnetic field. These effects were described theoretically by Dolgopolov and Gold for weakly disordered systems at low temperatures [130]. Two methods were used to extract $B_p$ - the magnetic field required to achieve full spin polarisation of the 2DHG. The first was simply finding where the shoulder occurred in the $\rho_{xx}$ data. The second followed a simplified method of that described by Yoon et al. [57]. In that report exponential functions were used to fit straight lines to $\log(\rho_{xx})$ vs in-plane magnetic field. Here straight lines were extrapolated from the regions shown in figures 6-6(ii) and 6-7(ii). The two regions correspond to the fully polarised (high field) and polarising (lower field) situations. Where these lines intersected for a given density was taken to be $B_p$. The $B_p$ are plotted against $n_h$ in the next section.
Figure 6-6: Sample A in-plane field data. (i) The raw data - note the noise present at lower densities. (ii) and (iii) Two different methods used to extract the magnetic field at which the holes are fully spin polarised.
Figure 6-7: Sample B in-plane field data. (i) The raw data. (ii) and (iii) Two different methods used to extract the magnetic field at which the holes are fully spin polarised.
6.3.4 Extracting $g^*m^*$

Figure 6-8 shows the $B_p$ obtained from figures 6-6 and 6-7 plotted as a function of hole density $n_h$. Values of $B_p$ for both 'arrow' and 'line' methods appear in figure 6-8 along with errors and straight line fits of the data. Errors in $B_p$ were determined for both fitting methods in the following manner. For the 'arrow' method a number of different attempts were made to plot the location of the shoulder in figures 6-6 and 6-7. A range in the magnetic field at which the turning point occurred would thus be generated which was used as the error in $B_p$. For the 'line' method a number of different lines were fitted to the data in figures 6-6 and 6-7 which created a range of magnetic field values over which the intersection of these lines could have occurred. This range was taken to be the error in the turning point of the $B_p$ associated with that particular intersection point. Substituting the gradients $\Delta B/\Delta n_h$ of the straight lines used to fit the data in figure 6-8 into equation 2.18 resulted in $g^*m^*$ of $2.22 \pm 4\%$ and $2.28 \pm 4\%$ for Samples A and B respectively. These are compared to literature values below.

Considering the dependence of $B_p$ on $n_h$, figure 6-8 shows that for low densities the fitted lines lie within the error bars of the experimental data. As the density is increased a difference arises between equation 2.18 and experiment because the density of states used in equation 2.18 neglects many-body effects between the holes themselves and any disorder present in the system [71].

6.3.5 Comparison with Literature

Comparing the $g^*m^*$ in the previous section with values in the literature is performed in this section. Starting with the (001) surface of a silicon transistor similar in structure to that used in these experiments, von Klitzing et al. found that $g^*m/m_0 = g^*m_{HH}^* = 2.34 \pm 10\%$ in 1974 where $m_{HH}^*$ is the heavy hole effective mass [131]. This is within $\approx 4\%$ of the values obtained in this experiment. This was determined using Klitzing et al’s heavy hole effective mass was of $0.47m_0$ [131]. Similar experiments in silicon by Dorozhkin et al. in 1989 demonstrated that the ratio of the $z$- and $x$-direction $g$-factors were $> 2.5$ for the (110) plane [132]. No absolute values of $g$ were given in that report.
Figure 6-8: Spin polarisation as a function of hole density for both Samples A and B.

Having demonstrated the determination of $g^*m^*$, data from [127] is now described along with the use of $g^*m^*$ in determining it's dependence on $n_h$ and the potential asymmetry within the quantum well $\delta n$. 
6.4 Controlling $g^*m^*$ With the Gates of a MOSFET

The values for $g^*m^*$ calculated above are combined with work by Niida [127] on similar silicon MOSFETs in order to demonstrate control of $g^*m^*$. A description of the experimental setup used by Niida and the ways in which it differed from the setup used above is presented below. This leads into a similar derivation of $g^*m^*$ as in section 2.5.1 but, due to the experimental setup, both the cyclotron and Zeeman splittings are considered. Niida’s data is then introduced and control of $g^*m^*$ demonstrated.

6.4.1 Niida’s Sample Orientation

Until this section, the MOSFET has been aligned either perpendicular or parallel to the magnetic field (figure 6-9(a)). This meant that both the cyclotron and Zeeman splittings changed with out-of-plane magnetic field while only the Zeeman splitting varied with in-plane field. In Niida’s work, the field perpendicular to the sample was maintained at 6 T while the in-plane component was varied by rotating the sample (figure 6-9(b)). This ensured that the cyclotron splitting $\Delta_C$ was constant while the Zeeman splitting $\Delta_Z$ was varied.

![Diagram](image)

**Figure 6-9:** (a) Data obtained at Grenoble and presented in this work corresponds to the case where the sample was either parallel or perpendicular to the applied magnetic field. (b) The experimental setup used by Niida allowed for the sample to be rotated in the magnetic field [127].

The next section considers the relationship between $g^*m^*$ and the ratio of $\Delta_Z$ to $\Delta_C$. Additionally, the different filling factors observed as $\Delta_Z$ is increased for constant $\Delta_C$ is described and is used to interpret data from [127].
6.4.2 The Zeeman and Cyclotron Splittings

In this section the derivation of the expression for $g^*m^*$ by considering the ratio of $\Delta_Z$ to $\Delta_C$ is presented. The major assumption underlying this derivation is that the out-of-plane $g^*$ was equal to the in-plane $g^*$. Additionally it was assumed that $g^*m^*$ was independent of magnetic field. From equations 2.22 and 2.16 the cyclotron and Zeeman splittings can be expressed as

$$\Delta_C = \frac{\hbar e B_\perp}{m^* m_0}, \quad \Delta_Z = g^* \mu_B B_{TOT}$$

(6.4)

where $B_\perp$ is the component of the magnetic field perpendicular to the 2DHG and $B_{TOT}$ is the magnitude of the field’s perpendicular and in-plane components; the other symbols have their usual meanings. The ratio $\Delta_Z$ to $\Delta_C$ can then be expressed as

$$\frac{\Delta_Z}{\Delta_C} = \frac{m^* m_0}{\hbar e B_\perp} \cdot g^* \mu_B B_{TOT}$$

(6.5)

and substituting for the Bohr magneton gives

$$g^*m^* = 2 \frac{\Delta_Z}{\Delta_C} \cdot \frac{B_\perp}{B_{TOT}}$$

(6.6)

There are certain requirements that must be fulfilled if equation 6.5 is to be applied to both the data from [127] and the previous sections in this chapter. Niida’s data and the necessary conditions are described in the next section.

If, as in [127], a constant perpendicular magnetic field is applied to the sample while the in-plane component of the field is increased, then the cyclotron splitting will remain constant as the Zeeman splitting increases. Figure 6-10 shows a schematic diagram of the appearance of the odd and even filling factors with increasing $\Delta_Z$ for a constant, non-zero $\Delta_C$ [70, 71]. When $\Delta_Z/\Delta_C$ is equal to an odd number, odd filling factors manifest while when the ratio $\Delta_Z/\Delta_C$ is equal to an even number, even filling factors appear. Data from [127] demonstrating the change in the filling factor with $\Delta_Z$ and $\Delta_C$ is shown in the next section. These data and figure 6-10 are used to interpret where with $\delta n$ and carrier density $g^*m^*$ changes.
6.4.3 The Dependence of $g^* m^*$ on Carrier Density and Potential Asymmetry of the Quantum Well

Data from [127] appears in figures 6-11(a) to (d) and shows the dependence of the second derivative of the conductance as a function of $n_h$ and $\delta n$. The diagonal magenta lines are used in later analysis. Although the perpendicular component of the magnetic field is constant throughout the figures, the in-plane component is increased from figure 6-11(a) to (d). This ensured that the cyclotron splitting remained constant whilst the Zeeman splitting changed with in-plane field. Also labeled on each figure are the minima associated with odd and even filling factors $\nu$. The filling factors can be observed to change with magnetic field for a constant density. Additionally, for constant in- and out-of-plane magnetic fields, the appearance of both odd and even filling factors is observable in figures 6-11(a), (b) and (d). In order to compare data in figure 6-11 with data from previous sections the following conditions must be met to ensure a fair comparison. First, the magnetic fields must be the same between datasets and secondly, the densities and asymmetry of the quantum well must also be the same between datasets. Similar magnetic fields occur when the out-of-plane field is equal to 6 T and the in-plane field is zero as used by Niida in figure 6-11(a). Additionally, similar densities and potential asymmetries must be used to try to ensure similar potential profiles within Niida’s 20 nm wide SOI layer and the 40 nm device used to determine $g^* m^*$. The density and $\delta n$ data from Sample A was used as this device did not have short-circuited gates. From Sample A’s data in
figure 6-4, at $V_B = 0$ V, $V_F = -4$ V, $n_h = 0.75 \times 10^{16}$ m$^{-2}$ and so $\delta n = n_F - n_B = 0.75 \times 10^{16}$ m$^{-2}$. Here the density contribution from the front gate $n_F$ was equal to $n_h$ because, at a back gate voltage of zero volts, the density contribution from the back gate $n_B$ was zero.
Figure 6-11: From [127]. The second derivative of the in-plane conductivity with respect to the hole density. The data are shown as functions of both \( \delta n_h \) and \( B_{\text{TOT}} \). Revealed in this is the development of the filling factors as \( B_\parallel \) is increased from (a) to (d).

Comparing these \( n_h \) and \( \delta n \) with figure 6-11(a) shows that that this point lies close to the
\( \nu = 5 \) minimum. As this is an odd filling factor it would be expected that the ratio \( \Delta Z/\Delta C \) was equal to some odd number (6-10). To determine what this number was, \( g^*m^* = 2.22 \) from Sample A’s data in figure 6-8 was substituted into equation 6.6 giving

\[
\frac{\Delta Z}{\Delta C} = 1.11 \tag{6.7}
\]

This value of \( \Delta Z/\Delta C \) fits with the odd filling factor of 5 observed in figure 6-11(a). However, both odd and even filling factors are present in figure 6-11(a). Changing \( \delta n \) and/or \( n_h \) changes the occupied Landau level and filling factor observed in the data. In order for \( \nu \) to change, the ratio in equation 6.7 was interpreted to be changing. From figure 6-10, the ratio \( \Delta Z/\Delta C \) must be approaching 2 having started at \( \Delta Z/\Delta C = 1.11 \). Using the coincidence method [21] and noting that the even filling factors are not very prominent compared to the odd \( \nu \), the ratio along the transition was thought to be 1.5. The magenta line represents where this transition was thought to occur; along the line itself \( \Delta Z/\Delta C \) would be constant. Errors for these lines are not shown in figure 6-11 for clarity. Substituting this value of 1.5 into 6.6 produced \( g^*m^* = 3.00 \).

Obtaining \( g^*m^* \) at the transition from odd to even \( \nu \), or vice-a-versa, from figures 6-11(b), (c) and (d) was achieved by using the coincidence method and figure 6-10 to discern what values \( \Delta Z/\Delta C \) might take. The ratios used were 1.5 for figure 6-11(b) and 2.5 for both figures 6-11(c) and (d). Substituting these values along with the relevant magnetic field values from each figure into equation 6.6 produced the \( g^*m^* \) values shown in figure 6-12. The solid lines in figure 6-12 correspond to the magenta lines in figures 6-11(a) to (d) with the relevant \( g^*m^* \) plotted for each line. The dotted lines of the same colour as their parent solid line in figure 6-12 represent the error in identifying the transition between odd and even filling factors in figures 6-11(a) to (d) occurred. The error in the \( B_{||} = 9 \) T was especially large as it proved difficult to identify where in figure 6-11(c) the transition between even and odd \( \nu \) occurred.

The dependence of \( g^*m^* \) on \( \delta n \) in figure 6-12 will now be considered. If, in figure 6-12, a constant hole density of \( 1.25 \times 10^{16} \) \( m^{-2} \) is set while increasing \( \delta n \), \( g^*m^* \) appears to increase rapidly between 2.48 and 3.00. The fact that \( g^*m^* \) increases with increasing asymmetry of the quantum well is most likely due to the simultaneous increase in confinement forced upon the holes. This increasing confinement drives the light and heavy hole subbands further apart in energy which in turn decreases the coupling between the light and heavy holes [71]. It was thought that the rapid rise in \( g^*m^* \) with \( \delta n \) was caused by the coupling between the hole species going to zero [18, 21]. The difference in quantum well widths in [127] and the samples used to determine \( g^*m^* \) was thought to affect the separation between the heavy and light hole subbands in the following way. For low \( \delta n \) the quantum well is symmetric and the coupling and mixing between light and heavy holes greatest because the splitting between their energy levels would be smallest. Increasing \( \delta n \) increases the confinement of the carriers and so forces the light and heavy hole subbands further apart in energy. This would act so as to reduce the coupling and mixing of the two hole species. This could have consequences for the application of the \( g^*m^* \) determined in the wider well to the data obtained in Niida’s narrower well.

These effects could be further tested experimentally by using quantum wells of different
widths to determine how $g^*m^*$ changes with confinement and $\delta n$. Additionally, the Schrödinger Poisson equations could be solved self-consistently as described in Chapter 2 for the heavy and light hole subbands for different quantum well widths, carrier densities and $\delta n$. A strong increase in $g^*m^*$ might be expected from these calculations for certain splittings between the light and heavy hole subbands. Additionally, the exchange interaction would need to be accounted for as this can enhance the effective $g$-factor, making it appear larger than it actually is when measured [48]; this was also discussed in Chapter 2. Also, the effect of in-plane magnetic field on the confinement of the holes needs to be considered for a fuller understanding of the data. As described by Kravchenko and Sarachik in their review paper [12], increasing in-plane field increases the confinement. As the in-plane field is increased in this experiment it would be expected that the increase in confinement would further reduce the light hole-heavy hole coupling and thus increase the measured effective $g$-factor.

![Figure 6-12](image_url)

Figure 6-12: The dependence of $g^*m^*$ on hole density and the potential asymmetry of the quantum well.

### 6.5 Conclusions

The demonstration of the dependence of $g^*m^*$ on the gate voltages of an Si-MOSFET was demonstrated utilising data from work by Niida Yoshitaka [127]. The rapid increase of $g^*m^*$ with $\delta n$ was attributed to the coupling between the light and heavy holes going to zero, leaving the heavy holes $g^*m^*$ and density of states dominating the properties of the system.
Chapter 7

An Introduction to Valley Splitting

7.1 Introduction

In this chapter the work conducted by Ouisse et al. and Takashina et al. on the discovery and subsequent study of giant valley splitting in Si-MOSFETs is reported. The initial identification of giant valley splitting in 1998 by Ouisse et al. [22], the further work by Takashina et al. in 2004 and 2006 [24, 29] are documented. Later in 2011 Takashina et al. demonstrated that there exists qualitative similarities between spin and valley polarisation on the transport properties of a 2DEG [40]; this is also discussed here. Additionally experiments performed by Niida et al. [128] that investigated the effect of the SIMOX BOX/SOI and FOX/SOI interfaces on the electron mobility are presented. The phenomenological model constructed by Takashina et al [133] to describe their experimental results is outlined. Finally, the model proposed by Koiller et al. [88] that attempts to explain the origin of giant valley splitting at the microscopic level is summarised.

The literature summarised in this chapter lays the foundations for interpreting work in chapters 8 and 9.

7.2 Chapter Overview

As the normal, small valley splitting was discussed in Chapter 2 it will not be considered here. Instead the discovery of its giant counterpart at the BOX/SOI interface of a Si-MOSFET by Takashina et al. is detailed [29]. Aspects of the model used to describe the giant valley splitting in that study are introduced but further analysis is delayed until after two other studies on the effects of giant valley splitting have been discussed. The first of these, also by Takashina et al., demonstrated qualitative similarities in the effects of valley and spin polarisation on the conductivity of the electrons within the silicon quantum well [40]. The model developed by
Takashina et al. to describe giant valley splitting is then fully introduced and extended to include the effects of spin polarisation on the system.

### 7.2.1 Important Definitions

The figure from chapter 2 is repeated below as it is used to identify some important quantities that will be referred to throughout this chapter. Considering when the system is valley degenerate both upper and lower valleys, (-) and (+) respectively, are equally occupied by the electrons 7-1(b)(i). A valley splitting $\Delta_V$ can be induced by applying an out-of-plane electric field to the electrons at the BOX/SOI interface. This decreases the occupation of the upper subband, eventually depopulating it completely and in doing so the system becomes valley polarised (figures 7-1(b)(ii) and 7-1(b)(iii)).

$$E = E_z$$

**Figure 7-1:** (a) From (i) to (ii): Confining the 6-fold degenerate system to a 2D plane lifts the degeneracy and gives rise to energy levels dependent upon the effective mass of the electron. (b) From (i) to (iii): An out of plane electric field is used to lift the valley degeneracy $\Delta_V$ of the 2-fold degenerate state. Under sufficiently large fields the electrons populate only the lower (+) valley at which point the system is said to be valley polarised.

### 7.3 Giant Valley Splitting

In this section a summary of the work by Ouisse et al. in [22] and Takashina et al. in [29] are presented. Data obtained by Ouisse et al. demonstrated the potential existence of giant valley splitting at the SIMOX BOX/SOI interface while the work by Takashina et al. confirmed its presence. Important aspects of the model Takashina et al. developed to describe the giant valley splitting are introduced but further explanation of this is delayed until section 7.4.2.

Figure 7-2(a) shows data from Ouisse et al. demonstrating a significant valley splitting at large back gate voltages when the 2DEG was close to the SIMOX BOX/SOI interface. This splitting was larger than had been previously observed but was not definitively explained by the authors of that work. Their consensus was that moving the electrons towards the SIMOX BOX 'switched on' a perturbing potential that coupled the two valley subbands and lifted the
valley degeneracy [22]. Attempts to model the splitting via a perturbative scheme showed that the valley splitting would be enhanced if a perfect interface was present and only one gate was active. The results of this calculation are shown in figure 7-2(b). The model failed to predict the size of the experimental values of the valley splitting in figure 7-2(a). Additionally it was demonstrated that the splitting could be further enhanced by applying a front gate voltage [22].

Figure 7-2: From [22] (a) Variation of the experimental valley splitting with back gate voltage. (b) The valley splitting calculated perturbatively from self-consistently solving the Schrödinger and Poisson equations in the SOI structure.

Whilst demonstrating the tunability of valley splitting via the gates of a Si-MOSFET, Takashina et al. demonstrated a potentially large valley splitting in their work published in 2004 [24]. Their results, displayed in figure 7-3, show that the valley splittings increase in magnitude as $\delta n$ is increased. They concluded that the valley splitting was strongly enhanced by the SIMOX BOX/SOI interface in accordance with the work described above by Ouisse et al.
Figure 7-3: From [24]. The valley splittings determined from Landau level coincidences at $\nu = 6$ hinted at much larger splittings at greater $\delta n$.

Giant valley splitting at zero magnetic field was first observed and reported on by Takashina et al. in 2006 [29]. Its effects on the conductivity of a 2DEG were measured as a ‘step’ in the $G_{SD}(V_F)$ characteristics (figure 7-4(a)).

Calculating the second derivative of $I_e(V_F)$ with respect to $V_F$ reveals features A, B and C as shown in figure 7-4(a). The development of these features with both front and back gate voltages is more clearly observed in figure 7-4(b). Feature A was found to occur over a range of gate voltages consistent with the calculated onset of electronic occupation of the second subband within the quantum well. Alternatively, for gate voltages above feature A, electrons
would then be present at both SOI/oxide interfaces. If a constant back gate voltage of 60 V is maintained while the front gate voltage is reduced from some positive value through A, a reduction in conductivity will be observed due to scattering processes as the subband edge as A is passed. Contributing also to the reduction in conductance is the fact that the electronic wavefunctions at either interface couple leading to a decrease in carrier mobility [29]. Further decreasing the front gate voltage continuously depopulates the electrons within the quantum well. Eventually feature B is crossed and a step is observed in the conduction characteristics of the 2DEG (figure 7-4(a)). Further reducing the front gate voltage stops conduction completely as C, the onset of conduction, is passed. It was thought that feature B arose due to the depopulation of the upper valley subband and that the region between B and C was valley polarised. To test this the sample was subjected to a magnetic field applied perpendicularly to the 2DEG. The magnitude of the field (5.5 T) was deliberately strong enough to induce a spin splitting but not spin polarisation of the electrons. The application of this field allowed the development of the periodicity of the Shubnikov-de-Haas oscillations to be monitored across the $(V_F, V_B)$ plane. For a spin split, valley degenerate system it was expected that the periodicity of the total filling factor would be $\Delta \nu^{TOT} = 4$ as this is the combined degeneracy of the spin and valley degrees of freedom. If the valley degeneracy were lifted between features B and C then the periodicity should have fallen to $\Delta \nu^{TOT} = 2$ as the only degeneracy left would be due to spin. Figure 7-5(a) shows the dark lines associated with minima in the Shubnikov-de-Haas oscillations while figure 7-5(b) plots calculated fits to these lines; the model used to predict these lines is discussed below. The strong, dark lines in the top left, valley degenerate region of 7-5(b) correspond to $\Delta \nu^{TOT} = 4$. Moving into the region bound by features B and C the lines have a periodicity of $\Delta \nu^{TOT} = 2$ which shows that the valley degeneracy has been lifted in this area on the $(V_F, V_B)$ plane leaving only the spin degeneracy. Moving into the region above B shows a criss-cross pattern of oscillations. Those parallel to B verified that this feature corresponded to the onset of occupation of the upper subband [29].
Figure 7-5: From [29]. (a) $d^2G_{SD}/dF^2$ at 5.5 T and 4.2 K. (b) The same data as (a) but with a different contrast. Solid squares are estimates of second spatial subband occupation. Solid straight lines show calculated lines of even $\nu^+$ and $\nu^-$ while dotted lines represent $\nu_{tot} = 4i$ where $i$ is an integer. The region enclosed by features C and B $(\nu^- = 0)$ is completely valley-polarized. (c) Density of states at zero magnetic field with and without valley splitting $\Delta_V$. (d) Resultant Landau levels. Thicker lines also correspond to valley subband edges.

To model $\Delta_V$ the empirical relation

$$\Delta_V = \alpha \delta n$$

was used where $\alpha$ was a fitting factor and $\delta n$ was the density contribution from the front and back gates given by $\delta n = n_B - n_F$. The definition of $\delta n$ was such that at positive $\delta n$ the 2DEG was closer to the BOX/SOI interface and would experience some quantity of the giant valley splitting. For negative $\delta n$ the 2DEG was closer to the FOX/SOI interface and so the giant valley splitting would be negligible. Thus for negative $\delta n$ it was assumed that $\Delta_V = 0$. To test it, the model was used to extract the filling factors for the upper and lower valley subbands, $\nu^-$ and $\nu^+$ respectively, in a valley-split system (figure 7-5(c)). The filling factors, given by $\nu^\pm = n^\pm/(eB/h)$ where $n^\pm$ is the carrier density in the upper and lower valley subbands, are plotted on figures 7-5(b) and (d).

Although this model would be extended to consider the effects of both valley and spin polarisation of the resistivity of a 2DEG, it would only happen after another experiment performed by Takashina et al. in 2011 [40]. This is detailed below.
7.4 Single Particle Effects of Spin and Valley Splitting in Two Dimensions

In this section the empirical model Takashina et al. used to explain their data in [29] is introduced and then extended to include the effects of spin polarisation as described by Takashina et al. in [40, 133].

7.4.1 The Valley-Split Subband Model

The model for the spin degenerate, 2-subband system in figure 7-5(c) was derived considering a single particle model at zero temperature. Each subband had a constant 2D density of states given by \( g(E) = D_0 = \frac{m^* m_0}{2\pi \hbar^2} \). Under valley degeneracy the energies of each subband \( E^+ \) and \( E^- \) would be equal and the densities within the subbands given by \( n^\pm = n_s/2 \) where \( n_s \) is the sheet density of the electrons. Introducing a small valley splitting \( \Delta_V \) leads to a subband separation given by \( \Delta_V = E^+ - E^- \). This valley splitting induces a density imbalance between the subbands where the density of each subband is given by

\[
n^\pm = \frac{1}{2} (n \pm D\Delta_V)
\]

Combining this and equation 7.1 leads to the relationship

\[
n^\pm = \frac{1}{2} [(1 \mp D\alpha)n_F + (1 \pm D\alpha)n_B]
\]

The model was tested by combining equations 7.1 and 7.3 with \( \nu^\pm = n^\pm/(eB/\hbar) \) allowing the fitting factors for the upper and lower valley subbands to be calculated. The results were plotted in 7-5(b).

The section below extends the simple 2-subband model shown here to include the effects of spin splitting as well as valley splitting. This model will be used in the coming Chapters.

7.4.2 The Valley- and Spin-Split Subband Model

Similar assumptions were used here as were used for the previous section. A simple system at zero temperature with a parabolic dispersion relation such that for a given spin-split, valley split subband the density of states is a constant \( g(E) = D_0 = \frac{m^* m_0}{2\pi \hbar^2} \) and the electron sheet density, given by \( n_s = D_0 E_F \), is considered. Additionally the electron sheet density is given by \( n_s = D_0 E_F \). Typical values for both the giant valley splitting \( \Delta_V \) and Zeeman splitting \( \Delta_Z \) were a few meV. Five cases arise from considering the effects of both valley and spin polarisation, \( \Delta_V \) and \( \Delta_Z \) respectively, on this system (figure 7-6) [133].
Figure 7-6: From [133]. The density of states in a 4-subband two dimensional electron system. The upper (+) and lower (-) valley subbands are split by $\Delta V$ while subbands of opposite spin are split by $\Delta Z$. Each spin-valley split subband labeled 1 to 4 has its own Fermi energy $E_1$ to $E_4$ defined as the energy difference between the Fermi level and the subband bottom.

The first case is simply when both spin and valley are degenerate giving $g(E) = 4D_0$ and $n_s = 4D_0E_F$. The second is when one of the subbands in figure 7-6 is empty, or when $g(E) = 3D_0$. Cases three and four occur respectively for fully valley or spin polarised systems such that $g(E) = 2D_0$ in both. Case five occurs when the system is both fully spin and valley polarised and $g(E) = D_0$. These regions and their boundaries are illustrated in figure 7-7 where $\Delta V$ and $\Delta Z$ are the axes on the parameter space.

Figure 7-7: From [133]. The density of states as a function of valley and spin splitting. The five cases with different density of states $g$ are marked as regions I to V. Key boundaries between them are marked - the boundaries were derived using equations in the body text.

The boundaries between regions in figure 7-7 can be derived by considering the density of states of each occupied spin and/or valley subband and the total density of the system. Only...
the boundary $AB$ will be considered here - the others can be found in a similar fashion. When the valley and spin splitting are both small, as in region I, all four spin and valley split subbands are occupied (figure 7-6):

$$n_s = D_0(E_1 + E_2 + E_3 + E_4);$$

$$E_2 - E_4 = \Delta_V;$$

$$E_1 - E_3 = \Delta_V;$$

$$E_3 - E_4 = \Delta_Z;$$

$$E_1 - E_2 = \Delta_Z;$$

$$E_2 - E_3 = \Delta_V - \Delta_Z;$$

$$E_1 - E_4 = \Delta_V + \Delta_Z.$$  \hspace{1cm} (7.4)

For each subband the Fermi energy is calculated as

$$E_1 = \frac{n_s}{4D_0} + \frac{1}{2}(\Delta_Z + \Delta_V);$$

$$E_2 = \frac{n_s}{4D_0} + \frac{1}{2}(-\Delta_Z + \Delta_V);$$

$$E_3 = \frac{n_s}{4D_0} + \frac{1}{2}(\Delta_Z - \Delta_V);$$

$$E_4 = \frac{n_s}{4D_0} + \frac{1}{2}(-\Delta_Z - \Delta_V).$$  \hspace{1cm} (7.5)

As valley or spin splitting is increased subband 4 will depopulate. Once $E_4 > 0$:

$$\frac{n_s}{4D_0} > \frac{1}{2}(\Delta_Z + \Delta_V).$$  \hspace{1cm} (7.6)

and so region I is bounded by the line when $E_4 = 0$:

$$\Delta_Z = \frac{n_s}{2D_0} - \Delta_V.$$  \hspace{1cm} (7.7)

As it was not specified whether spin or valley splitting was greater than the other the above equation is valid either way. Thus line $AB$ connects the points of valley polarisation under spin degeneracy (B) and spin polarisation under valley degeneracy (A) [134].

In this single-particle framework, the $(\Delta_Z, \Delta_V)$ diagram simply scales with density in such a way that figure 7-7 can be plotted as a function of $n_s$, $\Delta_Z$ and $\Delta_V$ (Top of figure 7-8). When $\Delta_Z = 0$ (figure 7-8(a)) only regions I and III are present while point B has become a line denoting the valley subband edge: $n_s = 2D_0\Delta_V$. Increasing $\Delta_Z$ splits this subband edge and region II emerges. The boundaries are defined by the equations shown in figure 7-8(b). Similar arguments were applied to the case when $\Delta_V = 0$ and $\Delta_V \neq 0$ resulting in figures 7-8(c) and (d).
In addition to the above it was convenient to define a spin and valley polarisation, $P_Z$ and $P_V$ respectively,

$$P_Z = \frac{n_+ - n_-}{n_+ + n_-}, \quad P_V = \frac{n_+ - n_-}{n_+ + n_-} \quad (7.8)$$

where $n_+$ and $n_-$ are densities of electrons with up and down spin respectively while $n_+$ and $n_-$ are densities of electrons in the lower and upper valleys respectively. These polarisations will be implemented in Chapter 8 when analysing spin and valley polarisation data. For comparison regions of the $(\Delta Z, \Delta V)$ parameter space are mapped to the $(P_Z, P_V)$ plane. Full
valley polarisation (region III, figure 7-9(a)) maps to the line BC in figure 7-9(b) while full spin polarisation (region IV, figure 7-9(a)) maps to the line AC in figure 7-9(b). Region V on figure 7-9(a) (full valley and spin polarisation) maps to point C on the \((P_Z, P_V)\) plane. The line AB in figure 7-9(b) separates the areas where the system is completely valley and spin degenerate (region I) and where one subband has been lifted above the Fermi level (region II). This line is given by the equation \(P_Z + P_V = 1\).

Figure 7-9: From [133]. (a) A line of constant \(P_Z = 1/2\) (thick dotted line) on the \((\Delta_Z, \Delta_V)\) plane. (b) The \((P_Z, P_V)\) plane with a line of constant \(\Delta_Z = n_s/4D_0\) (thick dotted line).

It is important to note that when considering the physics of the entire parameter space that the energies \(\Delta_Z\) and \(\Delta_V\) are not interchangeable with polarisations \(P_Z\) and \(P_V\). Table 7.1 shows the relationships between the valley and spin polarisations for regions I to V.

<table>
<thead>
<tr>
<th>Region</th>
<th>(P_V) and (P_Z)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>(P_V = 2\Delta_V D_0/n_s) [\text{and}] (P_Z = 2\Delta_Z D_0/n_s)</td>
</tr>
<tr>
<td>II</td>
<td>(P_V = \frac{1}{3} + \frac{D_0}{3n_s} (-2\Delta_Z + 4\Delta_V)) [\text{and}] (P_Z = \frac{1}{3} + \frac{D_0}{3n_s} (4\Delta_Z - 2\Delta_V))</td>
</tr>
<tr>
<td>III</td>
<td>(P_V = 1) [\text{and}] (P_Z = \frac{\Delta_Z D_0}{n_s})</td>
</tr>
<tr>
<td>IV</td>
<td>(P_V = \frac{\Delta_V D_0}{n_s}) [\text{and}] (P_Z = 1)</td>
</tr>
<tr>
<td>V</td>
<td>(P_Z = 1) [\text{and}] (P_V = 1)</td>
</tr>
</tbody>
</table>

Table 7.1: The valley and spin splittings for regions I to V.

The equations for region II contain both \(\Delta_V\) and \(\Delta_Z\) which shows that changing the energy
of one degree of freedom alters the polarisation of the other. For example, consider point A in figure 7-9(a) where \( \Delta Z = n_s/2D_0 \), \( P_Z \) is initially equal to 1. Moving up and away from point A increases \( \Delta V \) as Region II is traversed. Crossing the boundary to Region III on the midpoint of line \( BC \) means that \( P_Z \) has decreased by half to \( P_Z = 1/2 \). Thus valley polarisation has induced a spin depolarisation.

The equations in table 7.1 were used to calculate the polarisations \( P_Z \) and \( P_V \) in experiments reported on in both the next section and chapter 8.

### 7.5 Qualitative Similarities Between Valley and Spin Polarisation

In this section the temperature dependence of \( \rho_{xx} \) and its dependence on \( \delta n \), as reported by Takashina et al. in 2011 [40], are presented. The effect of a magnetic field on \( \rho_{xx} \) is then discussed.

Figures 7-10(a) and (b) plot the resistivity and temperature dependence of the resistivity respectively as functions of front and back gate voltage. Features A, B and C as found in figure 7-4 are visible here too although due to different oxide and SOI layer thicknesses they occur at different gate voltages. Also plotted over figures 7-10(a) and (b) are the carrier density and \( \delta n \) axes with certain values of both plotted on figure 7-10(a). If \( \rho_{xx} \) is plotted as a function of \( \delta n \) for a constant density a curious similarity with results in which \( \rho_{xx} \) is plotted as a function of spin-polarising, in-plane magnetic field is observed. Figure 7-10(d) demonstrates this similarity at \( \delta n = 0 \) [32]. For a review of magneto-transport in a range of material systems see the review paper by Spivak et al. published in 2010 [135]. Additionally Chapter 6 contains \( \rho_{xx} \) vs \( B_{||} \) data, albeit for holes not electrons. It was this similarity that lead Takashina et al. to conclude that both spin and valley polarisation had equivalent effects on \( \rho_{xx} \) [37, 40]. Pushing the analogy further, it was thought that a valley equivalent of the spin-Kondo effect should exist. Here that would be a ‘valley’-Kondo effect and could be observed by analysing the temperature dependence of \( \rho_{xx} \) (7-10(b)). In that figure the insulating feature just above B was thought to be due to localised electrons in the disorder broadened tail of the upper valley subband edge. These electrons would possess a spin degree of freedom and act as magnetic moments scattering electrons in the lower valley subband as per the Kondo effect in metals (figure 7-11) [136, 137]. These results were consistent with previous work by Feng et al. [137] on conventional Si MOSFETs in which it was reported that localised electrons do indeed enhance resistivity and that their presence acts so as to destroy metallic temperature dependence of the resistivity.
Figure 7-10: (a) to (c) are from [40] while (d) originates from [32]. (a) \( \rho \) at \( T = 350 \) mK. The thick black line labeled ‘upper valley subband edge’ corresponds to feature B in 7-4. Note that for \( \rho > 100 \) k\( \Omega \) the same colour as \( \rho = 100 \) k\( \Omega \) is used. (b) Change in resistivity between \( T = 0.35 \) K and \( T = 5 \) K where \( \Delta \rho = \rho(T = 0.35K) - \rho(T = 5K) \). For \( \Delta \rho > 10 \) k\( \Omega \) and \( \Delta \rho < -10 \) k\( \Omega \) colours for \( \Delta \rho = 10 \) k\( \Omega \) and \( \Delta \rho = -10 \) k\( \Omega \) are used respectively. (c) Resistivity at various densities \( n \) plotted as a function of \( \delta n \). Arrows mark the edge of the upper valley subband edge. Solid lines: \( T = 350 \) mK, dashed lines \( T = 5 \) K. (d) \( \rho_{xx} \) shows a similar trend as a function of in-plane field as it does when a function of \( \delta n \).

Evidence for the presence of localised spins along feature B was provided by analysing the in-plane magnetic field dependence of \( \rho_{xx} \). Figure 7-11(c) shows the change in resistivity between 15 T and 0 T such that \( \Delta \rho_{B||} = \rho(B|| = 15 \) T) - \( \rho(B|| = 0 \) T). Although figure 7-11(c) demonstrates the overall evolution of features A and B with magnetic field and density, it does not show the majority of the fine detail. Figure 7-11(d) allows the observation of the finer details of the dependence of \( \Delta \rho_{B||} \) on \( V_F \) at a constant \( V_B = 40 \) V. It is only at A and B in both figures 7-11(c) and (d) that negative magnetoresistance, or insulating behaviour, is observed.
This result was explained by considering the following. If there were no inter-valley subband interactions and both upper and lower valley subbands contributed independently to the conduction then only positive magnetoresistance would have been expected as in this case only the lower valley subband exhibits strong magnetoresistance. The fact that this was not observed suggested that the resistivity of the lower valley subband was enhanced due to the occupation of the upper valley subband edge at zero magnetic field and that this enhancement weakened at increased magnetic field [40]. Both orbital effects and coupling between the valley states and magnetic field were considered as potential alternative candidates to the spin degree of freedom. Orbital effects were eliminated [138, 139] as both valley subbands occupy the same confinement state in the quantum well which determines the out of plane envelope wavefunction. Coupling between the valley states and in-plane field was known to not occur as found by Wilde.
et al. [59]. This left spin as the remaining culprit for the observed negative magnetoresistance observed above feature B.

Ultimately, the findings of Takashina et al. suggested that an analogous effect should be present in in-plane field experiments of valley degenerate systems [140–143]. The already mentioned valley-Kondo effect should manifest in the spin polarisation of valley degenerate systems because electrons localised in the upper spin subband would be able to scatter electrons into the lower spin subband owing to the fact that they possess the valley degree of freedom. It was predicted that these localised valley moments would contribute an insulating temperature dependence to the resistivity when the Fermi energy lies close to the upper spin subband edge. Although observed by Lai et al. [140] in Si/SiGe systems and Si MOSFETs [142, 143] it was not covered in as much detail as in [32] - the paper upon which chapter 8 is based.

7.6 Electron and Hole Mobilities at thermal and SIMOX Oxide/Si Interfaces

The work conducted by Niida et al. [128] was done in an Si-MOSFET whose structure was similar to those used in the rest of this chapter. Electron and hole mobilities at both the thermal oxide/SOI and SIMOX BOX/SOI interfaces were measured and plotted as functions of $\delta n$ in figure 7-12 [128]. The data shows that the electron mobility was much lower at the SIMOX interface than the thermal oxide interface while the hole mobility at the SIMOX BOX/SOI interface was slightly higher than at the thermal FOX/SOI interface (figure 7-12). Two possible sources emerged for the observed mobility discrepancy. Either the disorder potential at the BOX/SOI interface produced a stronger effect on the electrons than the holes at the same interface or giant valley splitting, which the holes do not experience, was the culprit. To eliminate the disorder potential as a possible origin for these results Niida et al. first looked at the hole data. It was found that the out of plane potential confinement dependence of the hole mobility at the two interfaces produced similar results to the expected form for surface roughness scattering in a report by Tagaki et al. [144]. Niida et al. showed that for the holes the surface roughness scattering at the SIMOX BOX interface was weaker compared to that at the thermal oxide interface. This strongly suggested that the suppression of the electron mobility at the SIMOX interface was not due to an adverse magnitude of the surface roughness but dominated by the physics of valley polarisation itself [128]. In the electron data in figure 7-12(b) the arrows mark the boundary between partially valley polarised and, at higher $\delta n_e$, past the kink, fully valley polarised regions. This corresponds to feature B on figures 7-4(b) and 7-10.

A decrease in the $\mu_e$ data can be observed as $|\delta n_e| \to 0$ in both figures 7-12(a) and (b). This arises as $\mu_e$ is suppressed when $\delta n_e$ is small due to the effects of localised electrons in the upper spatial subband reducing the mobility of those in the lower spatial subband [48, 128]. This feature disappears as $|\delta n_e|$ increases due to the out of plane potential raising the confinement energy of the upper spatial subband with respect to the ground spatial-subband. It should be
noted that Niida et al. focus only on the transport properties where one spatial subband is occupied [128].

Figure 7-12: From [128]. All data obtained at 5 K. Both electron and hole densities were evenly stepped between 0.6 and $1.6 \times 10^{16}$ m$^{-2}$. (a) and (b) are respectively the electron mobility for $\delta n_e < 0$ and $\delta n_e > 0$ while (c) and (d) are respectively the hole mobility for $\delta n_h < 0$ and $\delta n_h > 0$. 
7.7 A Microscopic Model of Giant Valley Splitting

Although at present no theory can explain the magnitude of the giant valley splitting observed by Takashina et al. the work produced by Koiller et al. proposes a potential model [88]. Their theory is able to predict the large values of valley splittings as obtained by Takashina et al. These values were obtained by their demonstration that states in the conduction band hybridise with states in the Si/SiO$_2$ interface forming energy levels within the bandgap [88]. It is currently unknown why this hybridisation should occur at the buried oxide interface and not at the thermal oxide interface. The theory proposed by Koiller et al. may provide evidence for why this should occur; however, no attempt is made here to analyse why this might be. To demonstrate the role of hybridised states they define an interpolation parameter that describes the level of mixing where their $\alpha$ value varies between 0, for a pure conduction band state, to 1, a pure interface state. In figure 7-13(a) the five lowest energy eigenvalues calculated by their tight binding based model are shown as a function of $\alpha$. When $\alpha$ is small the levels present themselves as nearly degenerate doublets. These states are referred to Koiller et al. as valley states as they share an envelope. Thus they find it appropriate to equate the ground state gap to the valley splitting $\Delta_V$ [88]. For values of $\alpha$ in the range 0.5 – 0.8 the interface states were found to hybridise with the conduction band states and anti-crossings were subsequently observed. As can be seen from figure 7-13(a) the mixing only involves the lower of the two valley doublets which they take to be an indication of a valley selection rule [88]. For large $\alpha$ an interface state split off from the conduction band and extended into the band gap. Koiller et al do not attribute this to valley splitting as, although the ground state gap here becomes large, the wavefunctions of these two different states do not share an envelope [88]. The insets in figure 7-13(a) show probability densities of the electronic wavefunction for the lowest eigenstate for three different values of $\alpha$. The hybrid state at $\alpha = 0.70$ was found to exhibit characteristics of both the conduction band and interface states.
Until this point Koiller et al. have neglected the effects of disorder at the interface on their calculated valley splittings. The disorder here relates to vacancies and bending or stretching of atomic bonds across the Si/SiO₂ interface [88]. This disorder was modeled by assigning random values of \( \alpha \) to each position \( y \) along the interface in the range \([-0.26, \delta \alpha]\) while maintaining a constant \( \delta \alpha \) for all \( y \) in a given run. The value \(-0.26\) corresponded to the case where an oxygen atom was absent at the interface while the upper value \( \delta \alpha \) characterised the degree of
The ground state gap was shown to increase with $\delta \alpha$, eventually reaching values consistent with those found by Takashina et al. in 2006 for $\delta \alpha = 1$ [29, 88]. Additionally, the inset in figure 7-13(b) shows a histogram for the frequency distribution of the ground state gap for the disorder amplitude $\delta \alpha = 1$. Koiller et al. interpret the fact that $\Delta$ is always greater than 15 meV as indicating the enhancement of the ground state gap due to bond disorder [88].

7.8 Closing Comments

In this chapter the discovery of giant valley splitting by Ouisse et al. and Takashina et al. was described [22, 29]. Further to this, the discovery that spin and valley polarisations have similar, qualitative effects on $\rho_{xx}$ of a 2DEG was presented [40]. The qualitative model constructed by Takashina et al [133] to describe their experimental results was shown. Electron and hole mobility data from a study by Niida et al. [128] was included as the effects of the disorder potential of the SIMOX BOX/SOI and FOX/SOI interfaces on the carrier mobility are important in later chapters. Additionally work by Koiller et al. [88] concerning a potential model of the giant valley splitting observed by Takashina et al. was discussed. Ultimately the work summarised in this chapter is essential to interpreting work in chapters 8 and 9.
Chapter 8

The Effects of Spin and Valley Polarisation on the Resistivity of a 2DEG

8.1 Introduction

This chapter begins by presenting data that indicates a metal-insulator transition in quantum wells of widths 8 and 10 nm without an applied magnetic field. Additionally a dependence of the resistivity at zero field is shown to be dependent on the quantum well width. The chapter continues by considering the effects of a spin polarising magnetic field on the resistivity of a 2DEG with zero valley splitting. Building on this, valley polarisation of the 2DEG is shown to produce similar phenomenology on the electron resistivity as that produced by spin polarisation. This provides strong evidence for the equivalence of their roles in the underlying physics.

Much of the work in this chapter has already been published in [32].

8.2 Chapter Overview

The first half of this chapter details the effect of magnetic field on a 2DEG in two Si-MOSFETs with different quantum well thicknesses. This half begins with the dependence of the resistivity on temperature, electron density and quantum well width at $\delta n = 0 \text{ m}^{-2}$ and $B = 0 \text{ T}$. The evolution of $\rho_{xx}$ with magnetic field is then detailed at $\delta n = 0 \text{ m}^{-2}$. The magnetoresistance data is used as a foundation for the second half of the chapter that demonstrates how the giant valley splitting affects $\rho_{xx}$ in a similar manner to a magnetic field.

Although the background to the valley splitting itself was presented in Chapter 7, the MIT was not discussed. As that effect plays a prominent role in this chapter it is outlined in the next section.
8.3 The Metal-Insulator Transition

Here a brief history of the discovery and investigation into the MIT is detailed in preparation for analysis of data in the following sections. The results here demonstrate that the samples were working as described in the literature within the experimental areas of interest.

The scaling theory of localisation proposed by Abrahams et al. in 1979 suggested that no metallic state could exist in a 2DEG at zero magnetic field [145]. Although their model assumed a non-interacting system of particles, it was later shown in 1980 by Altshuler et al. that even weak interactions between the electrons further increased localisation [146]. In the opposite limit of strong interactions between electrons where a metallic state might be expected, it was predicted in 1989 by Tantar and Ceperley that even a small amount of disorder would force the system into an insulating state [147]. Experiments performed in the 1980s on 2D systems in a range of materials convincingly confirmed these predictions [148, 149]. However, in 1994 Pudalov et al. [150] and Shashkin et al. [151] discovered experimental evidence that there could indeed exist a metallic state of a 2DEG at $B = 0$ T. It was suggested that these results were due to the extended states of the Landau levels coalescing at the Fermi level and allowing for a metallic state of the 2DEG at $B = 0$ T [12]. Further studies of the temperature dependence on the resistivity of 2D carrier systems at $B = 0$ T revealed a metal-insulator transition; for a review see Kravchenko et al. [12]. This transition occurs at some critical carrier density below which the system exhibits increasing resistivity with decreasing temperature (insulating behaviour). For densities above the critical value the resistivity decreases with decreasing temperature (metallic behaviour). Additional work, such as that by Prunilla et al. [152, 153] demonstrated a similar transition of the resistivity with quantum well width. Both the MIT and the quantum well related transition are examined in the next section.

8.4 Resistivity as a Function of Temperature and Quantum Well Width at Zero Magnetic Field

This section introduces the samples used for experiments and outlines their differences. Experimental results demonstrating a MIT in the two quantum wells is then presented. A similar transition from high to low resistivity with carrier density was found to exist with changes in quantum well thickness. These results are also shown here.

8.4.1 The Samples

The structure of the MOSFETs used were like that shown in figure 3-1. Thicknesses of each layer are shown in table 8.1.
Table 8.1: *Layer thicknesses for samples A and B.*

<table>
<thead>
<tr>
<th>Sample</th>
<th>(d_{SOI} \text{ (nm)})</th>
<th>(d_{FOX} \text{ (nm)})</th>
<th>(d_{BOX} \text{ (nm)})</th>
<th>(W/L \text{ ((\mu)m)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>8</td>
<td>75</td>
<td>380</td>
<td>30/200</td>
</tr>
<tr>
<td>B</td>
<td>10</td>
<td>75</td>
<td>380</td>
<td>30/50</td>
</tr>
</tbody>
</table>

The experimental setup was the same for both samples. An AC voltage of 10 mV was applied to an n-type contact and the source-drain current through the sample measured as a function of front and back gate voltages. Densities were determined using an out of plane magnetic field up to 28 T in magnitude. In-plane magnetoresistance measurements revealed where a given density of electrons became spin polarised. To ensure the sample was either perpendicular to or parallel with the magnetic field, the same method as was described in Chapter 6 was used. In both cases \(V_{xy}\) was measured whilst aligning the MOSFET to ensure the correct orientation was achieved.

### 8.4.2 The MIT in 8 and 10 nm Wide Quantum Wells

The dependence of \(\rho_{xx}\) at \(B = 0 \text{ T}\) (\(\rho_{xx}(B = 0)\)) on temperature yields the results shown in figure 8-1. The data demonstrates trends presented in the literature [12] whereby the gradient \((d\rho/dT)\) changes sign at a critical density \(n_c\) at which \(d\rho/dT = 0\). It is this density that demarcates the metal-insulator transition where below \(n_c\) the resistivity shows an insulating temperature dependence with decreasing temperature. Above \(n_c\) the resistivity demonstrates a metallic dependence on temperature as \(\rho_{xx}\) decreases with decreasing temperature [12, 135]. In figure 8-1, \(n_c \approx 2.5 \times 10^{15} \text{ m}^{-2}\) for both samples A and B. The results in figure 8-1 are consistent with the wider literature.

![Figure 8-1: Temperature dependence of \(\rho_{xx}\) at zero field. Note that the lines are guides to the eye only.](image)

### 8.4.3 Dependence of the Resistivity on Quantum Well Width

Figures 8-2(a) and (b) show the dependence of \(\rho_{xx}(B = 0)\) on quantum well width \((d_{SOI})\) for \(T = 1.8 \text{ K}\) and \(T = 6 \text{ K}\) respectively. Qualitatively, there exists a similar dependence of the
resistivity on quantum well width and carrier density in figure 8-2(a) as the dependency of the resistivity on temperature and carrier density in figure 8-1. That is, below a certain density in figure 8-2(a) the resistivity increases with decreasing well width. Above this density the resistivity decreases with decreasing well width. The higher temperature data in figure 8-2(b) shows no such transition with only a decrease in the resistivity with decreasing well width observed for all densities. For the low density data \( n_e \leq 2.5 \times 10^{15} \text{ m}^{-2} \) in figure 8-2(a), it was thought that the increase in \( \rho_{xx} \) with decreasing well width was due to the following. At these densities the electrons were unable to effectively screen the disorder potential generated by the two Si/SiO\(_2\) interfaces. In the wider well the interfaces were further away from the 2DEG than in the narrower well. This meant that the effect of the disorder potential on the electron mobility was lessened in the wider well. In contrast, the electrons in the narrower well were closer to the oxide interfaces resulting in a greater detrimental effect of the disorder potential on the electron mobility and a subsequent increase in the resistivity [154, 155].

Moving to higher densities for a constant well width, the resistivity decreases as the electrons are better able to screen the disorder potential generated by the two oxide interfaces. The behaviour of \( \rho_{xx} \) with well width above electron densities of \( n_e = 3.0 \times 10^{15} \text{ m}^{-2} \) is similar to that observed by Prunnila et al. in [153] in a Si-MOSFET similar to the ones used here. In their report, Prunnila et al. demonstrated that the upper spatial subband became occupied for low carrier densities in wells at least 10 nm wide. Similar results were also observed by Takashina et al. in their 2006 study that included Si-MOSFETs with 8 and 10 nm wide quantum wells [156]. These results are returned because the difference in energy between the ground state and first excited state, the lower and upper spatial subbands respectively, is larger for smaller well widths. At the large densities in figure 8-2, only the lower spatial subband is occupied in the narrower well due to the large energy gap between the subbands [153, 156].

On the other hand, in the wider well the upper subband is closer in energy to the lower subband and so more readily occupied by the carriers. As the upper subband becomes occupied, localised electrons in the subband’s disorder broadened tail scatter carriers in the lower spatial subband. This adversely affects the electron mobility leading to an increase in the resistivity with increasing well width [153]. This effect can also be seen in a 40 nm wide well in figure 7-4 of Chapter 7.
Figure 8-2: (a) and (b) Dependence of $\rho_{xx}$ on quantum well width at zero field for two different temperatures. Note that the lines are guides to the eye only.

The transition in the behaviour of $\rho_{xx}$ with quantum well width and carrier density present in figure 8-2(a) is forced to a lower resistivity in figure 8-2(b). The density at which the transition occurs in figure 8-2(b) was beyond the density range of this experiment. The trend whereby the resistivity decreases with decreasing well width was earlier attributed to electrons becoming localised in the disorder broadened upper subband. At the greater temperature in figure 8-2(b) this broadening increases which means that the upper subband becomes populated at lower densities [153].

8.5 The Spin Polarisation of a 2DEG with Zero Valley Splitting

Resistivity is shown as a function of in-plane magnetic field for both samples in figure 8-3 at $\delta = 0$ m$^{-2}$. Each line of a given colour corresponds to a different electron density as listed in the legend. The dotted lines are $\rho_{xx}$ data at different temperatures. In the legend the temperature is shown in brackets for a constant density. Considering a constant temperature of 1.8 K, the dependence of $\rho_{xx}$ on the magnetic field $B$ and density is similar to work presented by Kravchenko and Sarachik in their review paper [12]. All the data at the lower temperatures demonstrate an increase in the resistivity as the magnetic field is increased. For lower densities this increase is especially large, hence the term giant magnetoresistance being used to describe it [12]. After this rise, a shoulder in $\rho_{xx}$ is passed and the resistivity plateaus (arrows on figure 8-3(a) and (b)). This shoulder is interpreted to occur when the electrons are fully spin polarised; the greater the electron density, the greater the magnetic field required to spin polarise them [12, 130]. As described in Chapter 6, the giant magnetoresistance is caused by the screening wavelength of the electrons increasing in response to the increasing magnetic field. These effects were described theoretically by Dolgopolov and Gold for weakly disordered systems at low temperatures [130].
Figure 8-3: Temperature and magnetic field dependence of $\rho_{xx}$. The arrows mark where full spin polarisation was estimated to occur. Solid lines demarcate different electron densities while the dotted lines are $\rho_{xx}$ data at different temperatures. In the legend the temperature is shown in brackets for a constant density. Note that the data at $n_e = 4.0$ and $4.5 \times 10^{16}$ m$^{-2}$ were obtained at 6.0 and 5.2 K for samples A and B respectively.

8.5.1 Spin Polarisation at $\delta = 0$ m$^{-2}$

Here the magnetic field required to spin polarise a given density of electrons, $B_P$, is detailed. Additionally, the magnetic field $B_C$ at which $\rho_{xx}$ at 1.8 K is equal to $\rho_{xx}$ at 6.0 K is presented. Both $B_P$ and $B_C$ are plotted as a function of carrier density for both samples A and B in figure 8-4. Also shown on figure 8-3 are the fields predicted by the single particle model ($B_{SP}^P$) when $g = 2.02$ and the mass is that of the free electron. The value of $g^* m^*$ used to fit data from samples A and B was 4.75 substituted into equation 8.1. This equation is repeated below, albeit rearranged for $B_P$

$$B_P = 2 \frac{n_s}{g^* m^*} \frac{h}{e}$$  \hspace{1cm} (8.1)
According to the data in figure 8-4, the magnetic field $B_p$ predicted by the single particle model is significantly greater than the fields determined from experimental data. This difference arises between the model and experiment because the density of states used in equation 8.1 neglects many-body effects between the electrons themselves and any disorder present in the system [71]. Considering the trend in $B_C$ with carrier density, it would appear that a decrease in well width forces the transition at which $B_C$ occurs to higher electron densities. This is consistent with data in figures 8-1(a) and (b) where the critical density at which the MIT occurs is forced to greater electron density in the narrower quantum well.
8.6 The Effects of Giant Valley and Spin Splitting on the Resistivity of a 2DEG

Continuing with data from sample A, the position of $B_P$ with increasing magnetic field and valley polarisation will now be considered. Although data for sample B was also obtained it was similar to that found with the narrower sample A. As a result of this similarity, sample B no longer appears in this Chapter. Much of the theory underlying the data analysis in this section was described in chapter 7 so is not repeated here. The single particle phase diagrams from that chapter are repeated below in figure 8-5 for ease of access.

![Diagram](image)

**Figure 8-5:** (a) Single particle phase diagram for a constant density $n$. $D_0$ still retains its definition of $m^*m_0/2\pi\hbar^2$. (b) A phase diagram in terms of polarisation. $P_V$ and $P_Z$ are respectively $(n_+ - n_-)/(n_+ + n_-)$ and $(n_\uparrow - n_\downarrow)/(n_\uparrow + n_\downarrow)$.

The different regions in figures 8-5(a) and (b) will be referred to while discussing the data.

8.6.1 In-Plane Magnetic Field Dependence of the Resistivity

Figure 8-6 shows the resistivity as a function of magnetic field for a range of densities and valley splittings. Figures 8-6(a), (c) and (e) were obtained at negative $\delta n$ ($\Delta V = 0$ m$^{-2}$) while figures 8-6(b), (d) and (f) were obtained at positive $\delta n$ ($\Delta V > 0$ m$^{-2}$). The Roman numerals on figures 8-6(c) and (d) correspond to the numbered regions on figure 8-5(a). Values of the valley polarisation $P_V$ are shown in figure 8-6 correspond to figure 8-5(b).

Starting with figure 8-6(a) at low electron density and $\Delta V = 0$ m$^{-2}$, a strong dependence of $\rho_{xx}$ on $\delta n$ is observed. This occurs because as $\delta n$ is made more negative the electrons are forced closer to the FOX/SOI interface. At this density the electrons are unable to effectively screen the disorder potential at this interface and so as the carriers are brought closer to it, the electron mobility decreases. The effects of this decrease in mobility are apparent in figure 8-6(a) where the resistivity rises rapidly with $\delta n$. The increasing effect of this disorder potential on the electrons can also be observed in the broadening of the shoulder in $\rho_{xx}$ [32]. Maintaining $\Delta V = 0$ m$^{-2}$ and moving to higher electron densities (figures 8-6(c) and (e)) the following effects were found. In contrast with the data in figure 8-6(a), the resistivity in figures 8-6(c)
and (e) was not as strongly dependent on $\delta n$. Although the electrons are again being forced closer to the FOX/SOI interface at increasingly negative $\delta n$, the greater density of carriers was able to better screen the disorder potential generated by this interface. As a result, the electron mobility remains greater here as is evidenced by the lower values of $\rho_{xx}$ in figures 8-6(c) and (e). A notable feature moving from figure 8-6(a) to (c) to (e) is that the absolute values of the resistivity are lower at higher electron densities than the $\rho_{xx}$ values at lower densities. The increased screening of the disorder at the front interface by the larger electron density leads to this phenomenon [32].

Moving on to $\Delta n > 0 \text{ m}^{-2}$, it was found that for figures 8-6(b), (d) and (f) at $\delta n < 0.75 \times 10^{16} \text{ m}^{-2}$ the dependence of $\rho_{xx}$ on magnetic field is similar to that found for the same $n_e$ in figures 8-6(a), (c) and (e). This is due to the electrons being far enough from the disorder-inducing potential at the SIMOX BOX/SOI interface to ensure that their mobility remains larger than it would if the carriers were closer to that interface. Increasing $\delta n$ forces the electrons closer to the SIMOX/BOX interface increasing the valley polarisation $P_V$. This means that even at large $n_e$ and $B = 0 \text{ T}$ the resistivity increases due to the greater effect of the mobility-reducing disorder potential at this interface. Returning to figure 8-6(b), a peak in $\rho_{xx}$ at $B \approx 15 \text{ T}$ can be observed for $\delta n = 2.00 \times 10^{16} \text{ m}^{-2}$. Increasing $n_e$ whilst maintaining this large $\delta n$ inhibits the appearance of the peak. The origin of the peak was thought to be related to the disorder at the SIMOX BOX/SOI interface for the following reason as the peak’s magnitude diminishes with increasing electron density. As already explained, a greater density of electrons is better able to screen the disorder potential at the SIMOX BOX/SOI interface. Additionally, the fact that the peak also decreases in magnitude with decreasing $\delta n$ as the electrons move away from the SIMOX BOX/SOI interface adds credence to the above argument [32].
FIG. 1: (a) Schematic diagram of the sample. (b) Dependence of valley splitting $\Delta V$ on $\delta n$. (c) Spin and valley split sub-bands. (d) Single particle phase diagram at constant density. (e) A 3d visualization of (d) with $P V$ as a further parameter. (f) A phase diagram in terms of polarization.

FIG. 2: Color online. Magnetotransport at $T = 1.4$ K as a function of $\delta n$. The left column (a), (c) and (e) shows data at negative $\delta n (\Delta V = 0, P V = 0)$ while the right column (b), (d) and (f) shows data at positive $\delta n$. Each row corresponds to different density where (a) and (b): $n = 2.5 \times 10^{15}$ m$^{-2}$, (c) and (d): $n = 3.5 \times 10^{15}$ m$^{-2}$ and (e) and (f): $n = 4.5 \times 10^{15}$ m$^{-2}$. For each density (row), identical colors are used for identical values of $|\delta n|$. Small arrows are guides to the eye, marking the shoulder feature described in the body text. $P V$ in parentheses [11] show values expected at zero magnetic field. Roman numerals in (c) and (d) show corresponding regions in fig. 1(d) where the dotted line boundaries are straight line guides to the eye joining points A, B and C.

FIG. 4: Color online. Temperature dependence of resistivity ($\rho_{xx}$: squares: $n = 2.5 \times 10^{15}$ m$^{-2}$, circles: $n = 4.5 \times 10^{15}$ m$^{-2}$). Data at $B = 0$ T are shown in the top row (a to e) while the lower row (f to j) shows data at $B = 28$ T. Each column corresponds to a value of $\delta n$ of $P (V, P S)$ for $n = 2.5 \times 10^{15}$ m$^{-2}$ is indicated in parentheses for each graph. Polarization at $n = 4.5 \times 10^{15}$ m$^{-2}$ is the same except in (d) where $P V = 0.87$ and (i) and (j) where the degree of spin-valley polarization is substantial but not full.

Figure 8-6: Development of $\rho_{xx}$ with in-plane magnetic field with and without valley degeneracy. Boundaries of the regions shown in 8-5(a) are shown in above (c) and (d).
Having described the effects of oxide interface disorder on the dependence of $\rho_{xx}$ on magnetic field and $\delta n$, other features present within figures 8-6(a) to (f) will now be discussed. As described in previous sections, the magnetic field $B_P$ at which full spin polarisation is interpreted to occur increases with increasing carrier density. This can be observed as the electron density is increased from $n = 2.5\times10^{15}$ m$^{-2}$ in figures 8-6(a) and (b) to $n = 4.5\times10^{15}$ m$^{-2}$ in figures 8-6(e) and (f). Additionally, $B_P$ also changes with increasing $\delta n$ as can be seen on figures 8-6(a) to (f). This effect appears largest for positive values of $\delta n$ as shown in figures 8-6(b), (d) and (f). The field at which $B_P$ occurs saturates with increasing $\delta n$ although in figure 8-6(f) this saturation has moved to magnetic fields beyond the range of the experiment. The saturation of $B_P$ with $\delta n$ was interpreted to occur when both full valley and full spin polarisation had been achieved [32]. However, according to the single particle model, under full valley polarisation ($P_V = 1$) the magnetic field required to achieve full spin polarisation doubles compared to the field needed to fully spin polarise a valley degenerate system ($P_V = 0$). The results in figures 8-6(b), (d) and (f) contradict this theoretical prediction although they are qualitatively consistent with previous measurements in AlAs systems [39, 157, 158]. This increase of $B_P$ by only a few Tesla was interpreted to be related to many body effects that are not accounted for in the single particle model [32].

The final feature to be discussed in the data presented in this section is related to point A in figures 8-5(a) and (b) and is marked by the arrow in figure 8-6(f). At this point the 2DEG is fully spin polarised whilst being valley degenerate ($P_Z = 1, P_V = 0$). In figure 8-6(f) the resistivity at the shoulder in $\rho_{xx}$ decreases very slightly for $\delta n < 0.5\times10^{16}$ m$^{-2}$. Increasing $\delta n$ beyond $0.5\times10^{16}$ m$^{-2}$ results in the shoulder regaining its dependence on $\delta n$ observed at lower electron densities. This decrease and subsequent increase of $\rho_{xx}$ with $\delta n$ might be explained in the following manner. Increasing $\delta n$ increases the valley splitting $\Delta V$ and so the system is forced away from A and into region II (figure 8-5(a)) where the system is both spin- and valley-split. The negative 'valley resistance' marked by the arrow in figure 8-6(f) was speculated to be associated with valley polarisation of localised states at the spin subband edge. This is analogous to starting at point B in figure 8-5(a) and then moving right by increasing the spin splitting $\Delta Z$. In this case, the spin polarisation of magnetic moments at the valley subband edge is observed [40, 136, 137]. However, no negative magnetoresistance is observed in figures 8-6(b) and (d) most likely because the electron density was too small in the experiment [32]. Where point A is concerned the negative valley resistance in figure 8-6(f) would correspond to the suppression of a valley Kondo effect mediated by localised valley pseudospin moments [40, 60, 159]. On the higher magnetic field side of the shoulder the single particle model predicts a transition from regions IV to II (figure 8-5(a)) with increasing $\delta n$. This would result in an increase in the density of states at the Fermi level and a decrease in spin polarisation. These would act to counter the effect of positive valley resistance from valley polarisation. Despite this, the resistivity is found to increase smoothly and monotonically with $\delta n$ except in the vicinity of A. It should also be noted that no strong feature in the magnetoresistance is observed as the boundary between regions I and II (figure 8-5(a)) is crossed [32, 126].
8.6.2 Temperature Dependence of the Resistivity

Here the temperature dependence of the resistivity at both a constant magnitude of $\delta n$ and varying electron densities is presented. Setting a constant $|\delta n|$ ensured that the magnitude of the disorder experienced by the electrons was the same, irrespective of which interface the carriers were closest to [32]. This allowed for a direct comparison of the effects of spin polarisation and valley polarisation on the electron resistivity. After demonstrating this similarity the global phenomenological dependence of the resistivity on valley splitting, spin splitting and temperature is considered.

Figures 8-7(a) and (b) show $\rho_{xx}$ as a function of temperature for $|\delta n| = 10^{16}$ m$^{-2}$ and $|\delta n| = 2 \times 10^{16}$ m$^{-2}$ respectively.

![Figure 8-7](image)

Figure 8-7: Comparison of the resistivity between spin-degenerate-valley-polarised and spin-polarised-valley-degenerate electrons at equal out of plane bias. Spin polarised data was taken at 28 T.

The data are also shown as a function of spin and valley polarisations $P_S$ and $P_V$ respectively. The data at full spin polarisation and valley degeneracy ($P_S = 1, P_V = 0$) were obtained at negative $\delta n$. The spin degenerate, valley polarised data ($P_S = 0, P_V = 1$) were recorded at positive $\delta n$. Maintaining a constant $|\delta n|$ ensured that the effect of the disorder potential from the oxide interfaces was the same irrespective of whether the 2DEG was closer to the FOX or BOX. Keeping the disorder potential generated by the oxide interfaces constant allowed for a direct comparison of the effects of spin polarisation and valley polarisation on the resistivity of the 2DEG. Consider figure 8-7(a) and the effects of spin polarisation and valley polarisation on carrier density for a constant $\delta n$ and constant disorder. For a given carrier density the dependence of $\rho_{xx}$ on the temperature is similar regardless of whether the system is spin or valley polarised. This similarity provides strong evidence that valley and spin polarisation play qualitatively similar roles in their effects on the resistivity. The same effect can be seen in figure 8-7(b) for a larger $|\delta n|$, adding weight to the above argument. Moving on to a more
general description of the data, consider both figures 8-7(a) and (b) at \( n_e = 2.5 \times 10^{15} \text{ m}^{-2} \). At this lower density it can be seen that for a given \( \delta n \) the absolute values of \( \rho_{xx} \) are similar. Additionally, at this low density, there is a noticeable difference in the temperature dependence of the resistivity between figures 8-7(a). For example, the low density resistivity data in figure 8-7(b) show a cross-over with temperature not seen in 8-7(a). A potential explanation for this is detailed below. For \( n_e = 4.5 \times 10^{15} \text{ m}^{-2} \), the dependence of \( \rho_{xx} \) on temperature is similar for both values of \( \delta n \). Additionally the absolute values of \( \rho_{xx} \) are similar at this higher density for \( P_S = 0, P_V = 0.87 \) and \( P_S = 1 \) and \( P_V = 0 \) in figure 8-7(a). There is, however, some discrepancy between the absolute values of the resistivity when the system is either valley degenerate and spin polarised or valley polarised and spin degenerate at \( n_e = 4.5 \times 10^{15} \text{ m}^{-2} \) in figure 8-7(b). These differences between the spin polarised, valley degenerate and spin degenerate, valley polarised data at constant densities could be caused by a number of factors. Firstly, there is no direct correspondence between the polarising value of the magnetic field used and the fully polarising ‘valley field’ to expect exact agreement between the two sets of \( \rho_{xx} \). Secondly, more physically fundamental differences between intervalley scattering and spin-flip scattering may well underpin the discrepancy described above [32].

Figure 8-8 presents a general description of the phenomenological dependence of the resistivity on valley splitting, spin splitting and temperature. The upper figures (a) to (e) present spin degenerate \( (B = 0 \text{ T}) \) data whilst in the lower figures (f) to (j) the electrons are spin polarised \( (B = 28 \text{ T}) \). The degree of valley splitting is varied from no valley splitting in the left-hand set of figures \( (\delta n = -2 \times 10^{16} \text{ m}^{-2}) \) to a valley polarised 2DEG in the right-hand dataset \( (\delta n = 2 \times 10^{16} \text{ m}^{-2}) \). Considering the case when \( \delta n = 0 \) and \( B = 0 \text{ T} \) (figure 8-8(c)), \( \rho_{xx} \) demonstrates metallic behaviour as the resistivity decrease with decreasing temperature for both densities [12, 135]. With negative \( \delta n \) the effect of the disorder potential from the FOX/SOI interface on the electron mobility increases as the 2DEG is forced closer to that interface. The reduction in mobility leads to the observed increase in \( \rho_{xx} \) at the lower density of \( n_e = 2.5 \times 10^{15} \text{ m}^{-2} \). Conversely, the higher density of \( n_e = 4.5 \times 10^{15} \text{ m}^{-2} \) retains the absolute values of \( \rho_{xx} \) and metallic temperature dependence displayed over the range \( \delta n = 0 \text{ m}^{-2} \) (figure 8-8(c)) to \( \delta n = -2 \times 10^{16} \text{ m}^{-2} \) (figure 8-8(a)). This retention was thought most likely to be due to the higher density of electrons being better able to screen the disorder potential at the front oxide interface [32]. Increasing \( \delta n \) towards \( 2 \times 10^{16} \text{ m}^{-2} \) (figure 8-8(e)) leads to a greater increase in the resistivity for both densities as the 2DEG undergoes full valley polarisation. Returning to \( \delta n = 0 \text{ m}^{-2} \) in figure 8-8(c) and then increasing the magnetic field to \( 28 \text{ T} \) results in an insulating dependence of the resistivity on decreasing temperature for both densities (figure 8-8(h)). This is a magnetic field induced transition to insulating behaviour driven by spin polarisation of the electrons [32]. Moving from figure 8-8(h) to figure 8-8(f) leads to a slight increase in the resistivity for the lower density of electrons. On the other hand, the higher electron density registers similar values and dependence of \( \rho_{xx} \) on the temperature for figures 8-8(h) to 8-8(f). Moving towards full valley and full spin polarisation (figure 8-8(j)) produces a marked increase in resistivity for both densities with an insulating dependence of the resistivity on decreasing temperature shown [32].
Figure 8-8: Temperature dependence of resistivity for two different densities; $n = 2.5 \times 10^{15}$ m$^{-2}$ (squares) and $n = 4.5 \times 10^{15}$ m$^{-2}$ (circles). The top and bottom rows are respectively 0 and 28 T while each column corresponds to a different value of $\delta n$. Polarisation ($P_S, P_V$) is indicated in parentheses for $n = 2.5 \times 10^{15}$ m$^{-2}$. Polarisation at $n = 4.5 \times 10^{15}$ m$^{-2}$ is the same except in (d) where $P_V = 0.87$ and (i) and (j) and where the degree of spin-valley polarisation is substantial but not full.

8.7 Conclusions

In this chapter the valley polarisation of a spin degenerate 2DEG was shown to produce similar phenomenology on the electron resistivity as that produced by the spin polarisation of a valley degenerate 2DEG. This was demonstrated by first introducing the overall dependence of the electron resistivity on both $\delta n$ and magnetic field. $\delta n$ was then maintained at a constant magnitude ensuring that the effect of the disorder potential generated by both thermal and oxide interfaces was the same on the resistivity of the 2DEG. This then allowed the similarity of the effects of spin and valley polarisation on $\rho_{xx}$ to be probed directly. A global picture of the temperature dependence of the resistivity with both magnetic field and $\delta n$ was also presented. From this global picture it was shown that the effects of both a spin polarising magnetic field and a positive $\delta n$ greatly increased the electron resistivity. This effect was more pronounced than that observed for the same field at negative $\delta n$. Additionally, data that indicated a metal-insulator transition with temperature in quantum wells of widths 8 and 10 nm without an applied magnetic field was shown. Finally, a quantum well width transition of the resistivity
with carrier density was found also evidenced by Prunilla et al. [152, 153].
Chapter 9

Suppression of Giant Valley Splitting by Reoxidation of the SIMOX BOX

9.1 Introduction

Differences in the thermal FOX and SIMOX BOX surfaces have been identified by Nagase et al. with atomic force microscopy after the SOI layer has been etched away [160]. Their results are reproduced in figure 9-1. Distinctive steps can be seen on the SIMOX box surface while the thermal FOX surface appears to be more random in its structure. It was thought by Dr. Akira Fujiwara that these step features may play some role in the size of the giant valley splitting observed at the SIMOX BOX/SOI interface. To test this, experiments were planned whereby MOSFETs with small front gate areas would be utilised to generate 2DEGs that overlapped as few of these steps as possible. By measuring the current as a function of gate voltage as described in Chapter 7, any variation in the magnitude of the signal B (figure 7-4), associated with giant valley splitting, with gate area could then be looked for in the data. As the step features in the SIMOX surface were of the order of 100 nm, it was suspected that some change in the giant valley splitting would occur at gate areas of this length and width. However, although B did get smaller and eventually go to zero with gate area, it was at the much greater order of micrometers, not the expected nanometers. As the data and reasoning in this chapter will show, this effect was thought to be caused by the reoxidation of the SIMOX BOX. A qualitative model is proposed to explain the disappearance of the giant valley splitting.

The work performed in this chapter was conducted at the Nippon Telegraph and Telephone Corporation in Japan.
9.2 Electrons at Thermal and SIMOX Oxide Interfaces

Although it has been proposed that the magnitude of the giant valley splitting can be affected by both atomic steps at the oxide/silicon interface [89] and the details of the potential at this interface [90] no practical work has yet been conducted to observe how control over these parameters can effect any change in the valley splitting. Images of the structure of the thermally grown oxide/SOI and SIMOX buried oxide/SOI interfaces provides evidence that differences exist between the two (figure 9-1) [160]. Although it could be argued that these exposed surfaces are different structurally compared to the actual oxide/SOI interface in an unetched MOSFET, some differences between the two are still evident in figure 9-1. The left hand image for both figures 9-1(a) and (b) is an atomic force microscope image of the relevant interface while the right hand images are cross-sections of those surfaces along the line AB. These cross-sections correspond to a length of 300 nm. Figure 9-1(a) shows the thermal FOX to be almost random in its structure while figure 9-1(b) shows the SIMOX BOX interface as being composed of a series of wide flat steps. These features have at least \( \approx 100 \) nm separating one surface from the next and a vertical step-height measurable in tenths of nanometers. It is interesting to note that these steps appear to arise in fractions of the silicon unit cell shown in figure 2-1.

![Figure 9-1](image)

Figure 9-1: From Nagase et al. [160]. (a) and (b) are thermal oxide/SOI and SIMOX BOX/SOI interfaces.

9.3 Experiment Objectives

Considering the results shown in figure 9-1 it was proposed that if a region of the SIMOX BOX/SOI interface were of the same order of magnitude in length (100 nm) as the flat steps
at that interface then some effect on the giant valley splitting may be observed. However, experiments would show that $B$, the feature associated with the depopulation of the upper valley subband (7-4), became zero at much larger SOI mesa sizes of the order of micrometers rather than the expected 100 nanometers. As discussed in chapter 7, giant valley splitting is an interface dependent quantity and should show no dependence on mesa sizes of this magnitude. Experiments then became concerned with why this had happened and used electron mobility data in figure 7-12(a) to interpret the results. The rest of this chapter details the results obtained and the qualitative model proposed to explain the results.

### 9.3.1 The Samples

In this section the physical structure and experimental layout of the samples are detailed. Important dimensions that dominate the conductance properties are shown.

The samples detailed here were dissimilar from others presented in this thesis. As stated in chapter 4 they were not Hall bars although they did possess the same cross-section as those samples shown in figure 3-1. Here the front and buried oxide thicknesses were respectively 20 and 400 nm for all samples in this chapter. Considering just the SOI mesa, the quantum well thicknesses were either 4 or 6 nm while the nominal mesa lengths and widths varied between samples as recorded in table 9.1 below.

<table>
<thead>
<tr>
<th>Sample</th>
<th>$d_{SOI}$ (nm)</th>
<th>Mesa width $W$ (µm)</th>
<th>Minimum width $W_{min}$ (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6.00 ± 1.96</td>
<td>200</td>
<td>50</td>
</tr>
<tr>
<td>2</td>
<td>4.00 ± 1.85</td>
<td>200</td>
<td>20</td>
</tr>
<tr>
<td>3</td>
<td>6.00 ± 1.96</td>
<td>10</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>4.00 ± 1.87</td>
<td>10</td>
<td>4</td>
</tr>
</tbody>
</table>

Table 9.1: Quantum well thicknesses and mesa widths. Note that all front and buried oxide thicknesses were 20 and 400 nm respectively.

Figure 9-2(a) shows a plan view of the general structure of the SOI mesa in each sample and the wiring used to probe the 2DEG at the SIMOX BOX/SOI interface while widths that dominate the conductance properties of the samples are shown in figure 9-2(b). The contact layout for each device used is shown in figure 9-3.
Figure 9-2: (a) The coloured regions indicate those areas degenerately doped with n- or p-type material. (b) Identification of important widths and lengths.

Three of the four samples, 2, 3 and 4, possessed the same physical layout as each other (figure 9-3). This made for a ready comparison of data between these devices. Owing to its different layout, Sample 1 utilised different contacts as shown in figure 9-3. As a result direct comparisons of data with this sample were not easy although qualitative comparisons were still possible.

Figure 9-3: Layout of the contacts used to perform experiments for the four samples.
For each Sample 1 source-drain voltage of 10 mV was applied to an n-type contact. The source-drain current would then be measured as a function of front gate voltage for a constant back gate voltage. The SMUs described in chapter 4 were used in experiments while pressures and temperatures of $\approx 10^{-7}$ Atmospheres and 6 K respectively were achieved via methods described in that chapter.

### 9.4 Comparing the Sample Data

In this section the source-drain current as a function of front gate voltage for different back gate voltages obtained from each Sample are detailed. Initially, it was thought that all Samples would exhibit the features reported by Takashina et al. in [29]. Those were the occupation of the upper subband (A), depopulation of the lower valley subband (B) and onset of current (C). As described in Chapter 7, it is the difference in $V_F$ between the peaks of A and B that is used to calculate the giant valley splitting.

![Quantum well thickness (nm)](image)

**Figure 9-4:** Here the overall trends observed in the data are considered. 100 V and 0 V were respectively the maximum and minimum back gate voltages applied to the samples.

However, despite the fact that all four samples were thought to possess SMIOX BOX/SOI interfaces, not all of the samples produced B, the feature associated with giant valley splitting. The data for all samples is shown below in figure 9-4. Reasons for the appearance, or absence, of A, B and C are described and explained. Figure 9-4 is laid out such that the left and right
columns contain data from the 4 and 6 nm quantum wells respectively. Minimum widths are shown within figure 9-4 for each sample.

Data from Sample 1 demonstrates all three features for large positive back gate voltages reported by Takashina et al. in [29]. Feature A has been forced to greater front gate voltages in Sample 2 due to the narrower quantum well possessed by this sample. This decrease in well width forces the upper subband to a greater energy and so a larger gate voltage is necessary to occupy it. Despite having a quantum well of the same width as Sample 1, A is absent from Sample 3’s data. For reasons explained later, it was thought that this absence was due to the quantum well actually being narrower than the nominal value of 6 nm. As with Sample 2, this would force the occupation of the upper subband to greater gate voltages due to the narrower well increasing the confinement energy of the upper subband. Where B is concerned Samples A, B and C exhibit it while D does not. In fact Sample 4 does not show any features associated with either the occupation of the upper spatial subband or giant valley splitting. The lack of the former can again be explained by the narrow quantum well in D pushing the upper subband to higher voltages while the absence of the latter was unexpected as D should possess a SIMOX BOX/SOI interface like the other samples. This progressive diminishing of B required an explanation as this feature is observed in Sample 2 which has a similarly narrow quantum well as D. The only physical, and immediately obvious, difference between samples B and D was the larger $w_{\text{min}}$ hosted by B. As the appearance of giant valley splitting is purely dependent on the presence of the SIMOX BOX/SOI interface it was reasoned that the decrease in the mesa width could not itself be eliminating B. Instead some other effect must have been responsible for the lack of this feature in Sample 4. Before describing the origin of this result, the data was subjected to further scrutiny. The second derivative of the source-drain current with respect to the gate voltage was calculated (figure 9-5) in order to observe any trend in the magnitude of the valley splitting across the samples used. Figure 9-5 shows that for the samples where giant valley splitting is present its magnitude does not noticeably change.

Figure 9-5 shows that Sample 4 is indeed the only sample to not demonstrate B. Conversely, Sample 4’s data possesses universal conductance fluctuations that are not present in data from Samples A or B and only just visible along C in Sample 3’s data (figure 9-5). The fact that these fluctuations are stronger in Sample 4 suggests that the reduction in size of the quantum well and SOI mesa was enough to reduce the number of available conductance channels in this sample leading to the observed fluctuations [18, 161]. This reduction in quantum well width may also mean that the electronic wavefunction interacts with the disorder potential at both interfaces due to the physical extent of the wavefunction throughout the well. Estimates of the extent of the wavelength depend on both the width of the well itself and $\delta n$. Under flat band conditions ($\delta n = 0 \text{ m}^{-2}$, figure 2-8(a)) the electronic probability distribution means the carriers are most likely to be found in the centre of the quantum well. Applying a gate voltage changes $\delta n$, increases the confinement and changes the width of the wavefunction (figure 2-8(b)). In the narrow wells described in this chapter the confined electronic wavefunction (as in figures 2-9(b) and (c)) was 2 nm in width; this value was obtained from a similar MOSFET used by Takashina et al. in [156]. The importance of the wavefunction width compared to the quantum
well width becomes more apparent when the error in the width of the quantum wells in table 9.1 are accounted for. This has ramifications for the appearance of giant valley splitting; these will be discussed in greater detail later. Although not obvious from figure 9-5, the positions and magnitude of B and C change with quantum well width. This is more obvious in the data plotted in figure 9-6 where the first and second derivatives of the source-drain current for a constant back gate voltage of 90 V are shown. The front gate voltage range used in figures 9-6(a), (b) and (c) shows the voltages over which giant valley splitting is observed in Samples 1 to 3.

Figure 9-5: The second derivative of the source-drain current. The units for the greyscale plots are $\mu SV^{-1}$. Note that the seemingly random data at the extremes of the $V_F$ range are artifacts of the calculation of the second derivative.

The magnitude of the peak responsible for B in figure 9-6(c) can be observed to change with quantum well width and $W_{\text{min}}$. Sample 1 possesses the largest signal associated with B followed by Sample 2 then Sample 3. Although B is absent in figure 9-6(c) for Sample 4, this Sample does possess a greater conductance $G_e$ in figure 9-6(b) than the other samples over a certain range of $V_F$. This range corresponds to the same gate voltages over which the giant valley splitting is observed in Samples A to C. This suggests that the electrons in Sample 4 have a greater mobility than those in the other Samples which would lead to the observed increase in the magnitude of the conductance. As was discussed in Chapter 7, the electron mobility is greater at a thermal oxide-SOI interface than at a SIMOX BOX/SOI interface [128]. For like densities Samples C and D should give the same $G_e$ because the carriers should have similar mobilities.
if the oxide interfaces are indeed the same in both samples. However $G_e$ is not the same in these samples, the fact that it is greater in the physically smallest sample over the region where giant valley splitting was expected suggested that the supposedly SIMOX BOX/SOI interface had somehow changed.

Figure 9-6: (a), (b) and (c) are respectively the source-drain current, transconductance and first derivative of the transconductance. All data is at $V_B = 90$ V.

9.5 Potential Methods by which the SIMOX BOX Became a Thermal Oxide

Here a method is proposed by which the SIMOX BOX became a thermal oxide. This is then applied to the samples reported on in this chapter.

The disruption of the SIMOX BOX/SOI interface into a different type of oxide interface could only have occurred during the thermal growth of the front oxide. After etching the SOI mesa as described in chapter 3, a number of surfaces of the SOI are exposed. The topmost is flat whilst the corners where the SOI and BOX join are non-planar; this is shown schematically in figure (figure 9-7(a)). Although the oxidation rate of a planar silicon surface was well described by the Deal-Grove model [117], it fails when the regions to be oxidised are less than 10 nm in size [162]. For length scales less than 10 nm the oxidation rate is strongly dependent on the size and shape of the structure, giving rise to the name PAttern Dependent Oxidation (PADOX) [163]. The join between the outer edge of the SOI mesa and the buried oxide produces a large mechanical stress at the interface of these two materials. As a result of this, the diffusivity of the gaseous oxygen in this strained region is increased allowing deeper penetration through this volume of BOX and into the SOI layer forming silicon dioxide at the backside of the SOI mesa.
This process of backside oxidation is shown schematically in figure 9-7(a) while figure 9-7(b) shows a TEM image of the back oxidation of an actual 20 nm thick, silicon quantum well. Each of the different layers in the MOSFET are shown here with the prominent effects of the back oxidation delineated by the arrow on the right hand side of figure 9-7(b). If this region were not oxidised then a rectangular shape SOI cross-section would be expected.

![Diagram](image)

**Figure 9-7:** (a) Schematic diagram of the growth of the front oxide and some of the oxygen penetrating the SIMOX layer resulting in the back oxidation of the SOI. (b) A transmission electron micrograph of a 20 nm SOI quantum well with the different layers shown. The oxidation of the extremity of the SOI is evident here. Some of the image has been removed, represented by the dotted line.

The following qualitative model was created to explain the lack of giant valley splitting in Sample 4 while considering the back oxidation method described above. The SOI layer in figure 9-7(b) was split into the two regions shown in figure 9-8. Region (i) pertained to the part of the quantum well that was at least the nominal thickness of the sample. This was also the location of the SIMOX BOX/SOI interface and the thermal FOX/SOI interface. Region (ii) was located where the back oxidation had occurred so that the quantum well was narrower than the nominal value and the SIMOX BOX/SOI interface had been replaced by a thermal oxide/SOI interface. Region (ii) was also assumed to maintain a constant width across all samples as all were made on the same wafer and so were subject to the same oxidation times. Where the electrons themselves were concerned, it was expected that a 2DEG in the quantum well would extend over both regions (i) and (ii). As these different regions were
formed of thermal and SIMOX oxides respectively, different conductance characteristics would be measured depending on the relative sizes of the two areas. If region (i) were much larger than region (ii) then the electron conductance would be affected primarily by the SIMOX oxide, producing a measurable value of $B$. On the other hand, if region (i) were smaller than region (ii) the conductance would be dominated by the characteristics of the thermal oxide and a smaller value of $B$ would be returned. Thus it was predicted that as region (i) reduced in size, $B$ would decrease in magnitude too. Additionally, as region (i) becomes smaller than region (ii), the average thickness of the quantum well will decrease. This will effect the appearance of A, B and C with respect to the front gate voltage. The data is described below in light of this model.

![Quantum well thickness (nm)](image)

Figure 9-8: Schematic of the SOI layers for each sample. Regions are identified where (i) the quantum well is at least the nominal thickness and a SIMOX interface is present and (ii) where the quantum well is less than the nominal value and the SIMOX BOX has been replaced by a thermal oxide.

The fact that $B$ decreases with decreasing quantum well thickness and $W_{\text{min}}$ can be explained as follows. In Sample 1 region (i) is larger than region (ii) so the conductance signal will be effected primarily by the SIMOX BOX/SOI interface in region (i). This gives rise to the large $B$ present in figure 9-6. Sample 2 evidences a smaller $B$ although this is unlikely to be caused by the smaller region (i) in this Sample as it is still significantly larger than region (ii). Here, the decrease in $B$ is most likely due to the decrease in quantum well thickness which brings the thermal FOX closer to the 2DEG. This means that, due to the extension of the electronic wavefunction across the quantum well, the disorder potential due to the FOX has an increased effect on the electron conductance. This reduces the magnitude of $B$ in figure 9-6(c). In Sample 3, $B$ is smaller again despite the nominally thicker quantum well which should reduce the effect of the thermal FOX on the 2DEG. Instead, this decrease of $B$ is explained in the following way. It was thought that regions (i) and (ii) were of a similar width in this Sample as $A$ was absent from Sample 3's data in figure 9-4. This absence could only be explained if the quantum well was thinner than the nominal value, which it would be on average if regions (i) and (ii) were of similar widths. Given also the errors in table 9.1 it is entirely possible that the quantum...
well was indeed thinner than expected. If the quantum well were on average thinner than the nominal value, the electrons would be affected by the thermal oxide interfaces at the front and in region (ii) thus further reducing the magnitude of B. In Sample 4, the effects described above combine to make the quantum well thinner on average than the nominal value of 4 nm. This means that the conductance is dominated by the effects of the thermal oxides in regions (i) and (ii) and so B is not observed in figure 9-6(c).

An alternative to the above theory is that, as demonstrated by Takashina et al. [29], the use of current as a probe for subband edges fails when disorder broadening brought on by increasing temperatures makes feature B increasingly difficult to discern. Although the temperature was low and constant throughout this experiment, the fact that B diminishes in size in smaller quantum wells suggests some similarity in the underlying physics. Disorder broadening from the close proximity of both oxide interfaces in the narrowest quantum wells would most likely be the cause of increased disorder leading to a broadening of the valley subbands and an apparent disappearance of the giant valley splitting.

To summarise, samples that were initially believed to contain SIMOX oxide interfaces and were used in an attempt to measure the giant valley splitting as a function of gate and SOI mesa area. Although B, the feature associated with the population of the upper valley subband, was found to go to zero, it was at mesa sizes of micrometers, not the expected nanometers. This effect was attributed to reoxidation of the SIMOX BOX/SOI interface which progressively reduced the magnitude of B as the quantum well thickness and minimum widths were reduced to nominal values of 4 nm and 4 µm respectively. The fact that the giant valley splitting could no longer be extracted from data in which the SIMOX BOX/SOI interface had been reoxidised supports the argument that giant valley splitting is related to the interface itself. It is, however, possible that using current as a probe for subband edges fails in sufficiently narrow samples where the disorder broadening from both oxide interfaces reduces the magnitude of feature B.

9.6 Conclusions

In this chapter it was shown that the feature associated with the occupation of the upper valley subband, B, was nullified by reoxidation of the SOI layer in samples where nominal the quantum well thickness was 4 nm and the smallest SOI mesa feature 4 µm wide. A qualitative model was proposed to explain the experimental results. Although these results could support the argument that giant valley splitting is related to the SIMOX BOX/SOI interface itself, it is also possible that the disorder generated by the thermal and SIMOX oxide interfaces in the narrower quantum wells render using the current as a probe for subband edges less useful for detecting giant valley splitting.
Chapter 10

Conclusions and Future Prospects

10.1 Introduction

In this thesis a variety of transport phenomena within a Si/SiO$_2$ MOSFET were studied. The areas investigated are summarised below and the main results detailed. Areas of future work and potential applications are also considered.

10.2 The Effects of a 2DHG (2DEG) on the I-V Characteristics of a 2DEG (2DHG) in a Bilayer System

A source-drain voltage in the range ±1 V was applied to a 2DEG or 2DHG in an electron-hole bilayer system. Depending on the densities of the carriers in each layer determined whether the G-V characteristics of the system returned that associated with a single-layer or $G_{e,h} \rightarrow 0$ S with no single-layer behaviour observed. Both the single-layer and bilayer characteristics were modelled to varying degrees of success. For certain source-drain voltages an inter-layer current was observed. This was attributed to a p-n like junction existing between the different carrier types. Potentially, this work could underpin efforts to create vertically coupled systems of charge carriers which could find use in novel electronic devices able to communicate both horizontally and vertically.

Future work could investigate the properties of excitonic states that would arise when individual electrons and holes form a bound state. It may be possible to modulate the electron spin within this state by altering the hole spin with one of the MOSFET’s gates. Control of the hole effective $g$-factor was demonstrated in Chapter 6. Additionally, this work could underpin efforts to investigate electron-hole drag in a bilayer system at high carrier densities as novel phenomena have been predicted under these conditions [53, 166–168]. However, a means of suppressing the inter-layer current must be found; a potential solution could be a device with
a structure like that used by Lattanzio et al. [169].

10.3 Control of $g^*m^*$ in a 2DHG on the Si (001) Plane with the MOSFET Gates

Control of $g^*m^*$ was demonstrated using the gates of the MOSFET hosting the 2DHG. The rapid change in $g^*m^*$ over a narrow range of $\delta n$ was attributed to the decrease, and eventual ceasing, of the heavy-hole light-hole coupling. As the coupling went to zero, the properties of $g^*m^*$ would then be dominated by the heavy holes only. Further work should include the calculation of the heavy-hole and light-hole energy levels and the coupling between the two states as a function of quantum confinement.

As described above, manipulating the hole spin via control of $g^*m^*$ in an excitonic state could potentially be used to study the effects of any amount of spin modulation in the electron layer. Although this has been proposed on a theoretical basis by Kumar et al. [45], it has yet to be experimentally tested. Additionally, this work provides a step towards the spin-modulating transistor proposed by Datta and Das [17]. Devices like this would extend Moore’s Law as they utilise another degree of freedom available to the charge carriers [6].

10.4 Giant Valley Splitting

The effects of giant valley splitting on the resistivity of a 2DEG were shown to be phenomenologically similar to the effects of a spin polarising, in-plane magnetic field on the resistivity applied to the same, valley degenerate 2DEG. From a technological point of view, this could form the basis of investigations into a device that utilises the valley degree of freedom instead of just charge, as in traditional transistors, or spin, as in spintronic devices. Further work in this area includes an investigation into the ability to force spin depolarisation by using the valley degree of freedom [170]. Additionally, it is thought to be possible to utilise the giant valley splitting to convert the silicon in these Si/SiO$_2$ MOSFETs into a direct bandgap. However, this is yet to be demonstrated in the literature.

It was shown that the feature associated with the occupation of the upper valley subband, B, was nullified by reoxidation of the SOI layer in samples where the nominal quantum well thickness was 4 nm and the smallest SOI mesa feature 4 $\mu$m wide. A qualitative model was proposed to explain the experimental results. These results support the argument that giant valley splitting is related to the SIMOX BOX/SOI interface itself. However, further work is required to determine if the giant valley splitting is in fact still present as it could be that using current as a probe for subband edges fails within the narrowest quantum wells due to disorder broadening of the valley subbands [29]. Future work could not only minimise the effect of wrap-around oxidation, but also use some other method of investigating whether the giant valley splitting was still present within the smallest devices. This could be achieved utilising an optical method as described above.
Attempts to manufacture MOSFETs from CZ wafers hosting front and back SIMOX/SOI interfaces failed due to a short circuit between the device gates and the SOI mesa. This was caused by over-etching of the spin-on-glass layer revealing the SOI. This could be resolved in future work by using an anisotropic etching technique, such as a reactive ion etch, that would create holes with vertical sides in the spin-on-glass layer. Devices such as these could be used to demonstrate giant valley splittings at smaller gate voltages than those found by Takashina et al. in [29]. This would reduce the power consumption of the samples and make them potentially viable for technological applications. This could lead to a new field of valleytronics in which transistors utilise the valley degree of freedom and so extend Moore’s Law [6, 28].
Appendices
Appendix A

Silicon MOSFET Fabrication at the University of Bath

A.1 Introduction

In this appendix the attempts to fabricate working Si-MOSFETs at the University of Bath are detailed. The fabrication process is outlined and explained. Although the initial experimental purpose for the MOSFETs was to measure giant valley splitting at the front SIMOX oxide/SOI interface within these samples, no functioning samples were realised. Reasons for this failure and improvements to the production process are suggested for future work.

A.2 The Valleytronics Wafers

In this section the wafers used for the fabrication process are introduced and their structure described. The naming convention for each cleaved section of the wafer is shown and the photomask used during the photolithographic steps is introduced and its layout outlined. The wafers used in this study were fabricated by Dr. Takashina at the Nippon Telegraph and Telecommunications Corporation based in Japan. These 'Valleytronics' wafers possessed the cross-sectional structure shown in A-1(a) with layer thicknesses displayed in table A.1. Two SIMOX oxide/SOI interfaces existed in these wafers instead of just the SIMOX BOX/SOI interface as found elsewhere in this thesis. To create the SIMOX front oxide the SIMOX process described in Chapter 3 was performed in place of the thermal oxidation step typically used to grow the front oxide. Prior to the formation of the new SIMOX interface, an etch back of the SOI layer was performed; again using methods described in Chapter 3.

As this new SIMOX oxide was significantly thinner than the back SIMOX oxide lower voltages could be applied to the front gate to produce the same giant valley splitting that would otherwise only be obtainable at large back gate voltages. These lower voltages would make investigating the giant valley splitting easier and less likely to result in broken samples.
Additionally, if any practical application of giant valley splitting were to be implemented, lower gate voltages would be necessary in order to reduce the power used by the transistor.

As the wafers were already fully formed the entire fabrication process described in Chapter 3 could not be followed. Instead structures had to be etched out of the wafer surface using the etching and photolithographic steps described in that chapter. Additionally low temperature doping techniques that did not disrupt the front SIMOX/SOI interface were also a requirement. The electron and thermal evaporating processes described in Chapter 3 were used for this particular step.

![Figure A-1: (a) A schematic cross section of the valleytronics wafers. (b) The final product.](image)

The five valleytronics wafers in table A.1 possessed different layer thicknesses with some layers missing entirely. Wafer A had no polysilicon deposited to allow for potential fabrication on top of the wafer. D1 and D2 were used for practicing photolithography, determining etch rates of the chemicals used and metal deposition processes.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Poly-silicon</th>
<th>Front SiO₂</th>
<th>SOI</th>
<th>Back SiO₂</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0</td>
<td>2316</td>
<td>1043</td>
<td>3873</td>
</tr>
<tr>
<td>B</td>
<td>1830</td>
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<td>1061</td>
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<td>1830</td>
<td>2253</td>
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<td>3843</td>
</tr>
<tr>
<td>D1</td>
<td>1830</td>
<td>1150</td>
<td>Bulk</td>
<td>0</td>
</tr>
<tr>
<td>D2</td>
<td>1830</td>
<td>1150</td>
<td>Bulk</td>
<td>0</td>
</tr>
</tbody>
</table>

Table A.1: The thicknesses of the different layers within the valleytronics wafers. All units are in Angstroms.

In order to process them the wafers had to be cleaved into smaller components. The manner in which this was performed is discussed later while the names for each cleaved section are described below as these will be referred to throughout the rest of the chapter.

**A.2.1 The Wafer Naming Convention**

Figure A-2 shows schematically how the wafers would be cleaved. Each part is named where A-2(i) was the wafer itself, A-2(ii) a chip, A-2(iii) a sub-chip and A-2(iv) the one or sometimes two samples that would be present on the sub-chip.
In order to etch the top three layers in figure A-1(a) the photolithographic and etching techniques described in Chapter 3 were implemented. For the photolithography a photomask was required; this item is detailed below.

A.2.2 The Photomask

A quartz photomask containing 5 active regions was obtained for use with the UV mask aligner. Each active region contained a blueprint that would allow that 2D structure to be imprinted onto the surface of a resist covered chip. The active regions are represented schematically in figure A-3(a). Figure A-3(b) shows the 16 samples that were to be fabricated using each active layer in a specific order shown on figure A-3(a). This order will be referred to when the fabrication process is described. Each of these areas possessed a design that was transparent or opaque to UV radiation in specific regions. While figure A-3(a) shows only the designs for a 2-terminal transistor many others were present within a given active region (figure A-3(b)). Each active area was 1 cm$^2$ in size allowing for a sample spacing that ensured there was no risk of the MOSFET designs overlapping each other.

When using the mask aligner, the resist coated chip would be placed on the chuck of the mask aligner and brought into contact with one of the active regions on the photomask. Exposure to UV radiation would then commence as shown in figure A-3(c).
Figure A-3: (a) A plan view of the five active regions on the photomask. Black areas were opaque to the UV radiation. The numbers above each active region correspond to the order in which they were used while the pictures within each active region represent the designs used in the creation of a 2-terminal MOSFET. (b) An active region showing the sixteen device locations. The numbers denote how many source-drain contacts the samples have while CD corresponds to Corbino disks. The two-terminal sample in the bottom right corner was considerably larger than the others and so was isolated from them. (c) A cross-section of the photomask and one of the active regions positioned over a resist covered chip (red). The chip is being exposed to ultraviolet radiation in the figure.

A plan view of the desired structures with nominal SOI mesa widths, lengths and in the case of the Corbino disks, radii are depicted in figure A-4. The aluminium contacts have been omitted so that the mesa itself can be focused on. A short distance between the SOI mesa and the poly-Silicon gate arose due to overetching. This was never larger than 2 µm on either side.
Figure A-4: For all samples the widths and lengths of the SOI mesa ($W_{MESA}$ and $L_{MESA}$ respectively) under the poly-Si front gate are shown in dotted red. $W_{MESA}$ and $L_{MESA}$ are shown for all samples. $r$ and $\Delta r$ are used for the Corbino disks. The length of the connecting wires ($L_{WIRE}$) was at least 100 $\mu$m for all 5 and 12 terminal samples. Doped regions are shown in yellow. (a) Two terminal devices. (b) Five terminal samples. (c) Twelve terminal samples. (d) The Corbino disks.
A.3 Sample Fabrication

This section covers the major steps of the MOSFET fabrication in the University of Bath’s class 10,000 cleanroom. The fabrication process included the following steps: cleaving and cleaning of wafers and chips, SOI mesa definition utilising photolithography and etching techniques, silicon doping and formation of the aluminium contacts and back gate. Each of these is described below while figure A-5) shows a schematic diagrams of the major processes involved in creating a 2-terminal MOSFET. Full details of each step can be found in the process sheet in Appendix B.

A.3.1 Cleaving and Cleaning

The wafers themselves were of the size shown in figure 3-1(b) and needed to be cleaved in order to be of a suitable size for processing. This was performed using a diamond scribe to cut the wafers into 1 cm$^2$ pieces, a size that ensured they were easy to handle with tweezers and allowed for at least 10 samples per chip. Once cleaved into chips any detritus on their surfaces had to be removed to ensure no defects were present that would disrupt the subsequent steps. Chips were cleaned by immersion for 10 minutes in Piranha solution; a mixture of 3:1 hydrogen peroxide to sulphuric acid. A 10 minute rinse in de-ionised water followed to remove any remaining acid.

A.3.2 Mesa Definition: Photolithography and Wet Etching

The mesa in (figure A-5)(a) was created using a combination of wet etching and active region 1 (figure A-3(a)). These processes are described in this section.

To selectively mask the chip against the wet etchants, photoresist Shipley 1813 was spun onto the chips using a resist spinner. This would immediately be followed by prebaking the chips at 90 °C for one hour to cure the resist. Active region 1 would be used in conjunction with the mask aligner and, once aligned over the resist covered chip, exposed to UV radiation for approximately 5 s. Immersing the chip in 351 solution for 30 to 40 s developed the regions exposed to the UV. The exposed polysilicon was etched away with a solution of 20:1:10 Nitric acid to Ammonium fluoride to DI Water (NAW solution) with the front oxide acting as an etch-stop. Etch rates for this solution were obtained from [171] and measured using the dummy wafers. After the NAW etch the chip would be rinsed in DI water, dried with nitrogen gas and then immersed in a buffered oxide etchant (BOE). This was a solution of hydrofluoric acid and ammonium fluoride; the ammonium fluoride controlled the etch rate of the hydrofluoric acid [171]. The etch was stopped by the SOI layer as BOE does not etch silicon. Again, etch rates for this were measured using the dummy wafers. After the FOX had been etched the chip would again be rinsed and dried as above before being immersed in NAW solution to etch away the SOI.

The measured etch times for the different layers of each wafer and each etchant can be found in table A.2 while full details of their determination are described in Appendix B.
Table A.2: The etch times of the different layers within the valleytronics wafers. All times are in seconds.

The times presented in table A.2 are the bare minimum that the chips would be subjected to a given etchant. It would sometimes be necessary to immerse the chip for slightly longer in a given solution to completely remove that layer. When etching either of the polysilicon or SOI layers a colour change would be observed as the silicon was removed. The colour would cease to change once the silicon etched away completely. To determine if the front oxide had been completely removed the chip would be submersed in NAW solution. If no colour change was observed then some oxide remained and the chip would be left again in the BOE for a further 20 s. This process would be repeated if needed. Note that the chip would be rinsed and dried as previously described between being immersed in either NAW or BOE to prevent cross contamination. The final mesa is shown in figure (A-5(a)).

Figure A-5: A schematic diagram of the major steps in the fabrication process. From top to bottom we see the photoresist (red), poly-silicon (grey), front FOX (white), SOI (grey) and the back BOX (white). (a) The etched mesa with the resist acting as a protecting mask against the etchants. (b) The shaped front gate and the front FOX. (c) Lift-off most of the AuSb except for that on the SOI. The dotted lines show the FOX holes to the SOI. (c) The finished sample with aluminium contacts. For clarity the full extent of the SOG has been omitted.
A.3.3 Doping the SOI

With the mesa defined, the next step involved creating a self-aligned gate and doping the SOI such that it became n-type. To begin this process any resist remaining on the chip from the previous processing was removed with acetone before the resist-spinning steps described above were used to again cover the chip in photoresist. After curing the resist, active region 2 (figure A-3(a)) and 351 solution would be used to respectively expose and develop regions of the polysilicon that were to be etched with NAW solution. After etching the polysilicon the FOX was exposed and front gate formed as shown in figure A-5(b). Any remaining photoresist would be removed and new resist spun and cured on the surface of the chip. In order to dope the SOI holes in the FOX were required. Active region 3 was used to expose areas of the FOX above the SOI that were to be etched. After development with 351 solution a BOE revealed the SOI and in doing so created the FOX-holes shown in figure A-3(c). These holes were positioned such that the later evaporation would deposit material onto both the SOI and polysilicon front gate. This ensured a self-aligned gate would be created once the dopants were activated. If the gate were not self-aligned, the device would either not work (figure A-6(a)) or there would be capacitive problems between the doped regions and the gate (figure A-6(b)). The case in figure A-6(b) could also lead to a short circuit between source-drain contact and front gate as the later evaporation of the contact metal might detrimentally overlap the two regions.

After the BOE the n-type dopant AuSb was evaporated onto the resist covered chip as soon as possible to prevent the growth of an insulating native oxide. AuSb was used because it thermally activated in silicon at 350 °C [102]. The evaporation was performed using a thermal or electron-beam evaporator to deposit 80 nanometres of material. This dopant thickness ensured that enough material would diffuse into the SOI in later stages whilst also minimising the chances of a short circuit between contact and front gate as the FOX was at least 225.3 nm thick.

After the evaporation AuSb would cover both the desired areas of SOI and the rest of the resist covered chip. To remove this excess AuSb the chip was submerged in acetone and subjected to ultrasonic vibrations. The vibrations removed loose material while the acetone removed resist and AuSb present on its surface. This process, known as lift-off, created the golden regions in figure A-5(c).
A.3.4 Spin-on-Glass (SOG) and Aluminium Wiring

To contact the doped regions of the SOI required metal contacts to those regions. Aluminium was the material of choice as it is a good conductor, adheres well to silicon dioxide and was cheap and readily usable with the evaporators. However, if the metal were evaporated directly onto the chip it risked overlapping the gate and SOI, creating a short circuit that would ruin the transistor. To prevent this happening spin-on-glass (SOG) was used to act as an insulator between the aluminium and the SOI. SOG is so named because it can be used with photoresist spinners as was the case in this report. Flowable oxide 25 from Dow Corning was used as once cured it would produce an 800 nm thick layer of oxide. The curing process was determined using information from the instructions supplied by Dow Corning and work by [172, 173] and fruitful discussions with Dr. M. Hopkins and other SOG users. To cure the SOG the times and corresponding temperatures shown in table A.3 were used.

<table>
<thead>
<tr>
<th>Step</th>
<th>Temperature (°C)</th>
<th>Time (minutes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>74</td>
<td>10</td>
</tr>
<tr>
<td>2</td>
<td>150</td>
<td>10</td>
</tr>
<tr>
<td>3</td>
<td>200</td>
<td>10</td>
</tr>
<tr>
<td>4</td>
<td>300</td>
<td>10</td>
</tr>
<tr>
<td>5</td>
<td>400</td>
<td>60</td>
</tr>
</tbody>
</table>

Table A.3: The curing regime for the SOG.

The temperature of the hotplate used for this process would be increased by roughly 20 °C every 30 s until the desired temperature for a given step in A.3 was achieved. Although time intensive, this ensured that there was minimal cracking in the cured SOG due to temperature shock. The process also caused the AuSb to diffuse into the SOI and activate; thus creating n-type regions in the silicon.

To contact the doped SOI with aluminium, holes through the SOG were created using the following method. After spinning and curing photoresist on the chip, active region 4 of the photomask was used to expose regions of SOG above the doped SOI and polysilicon gate. Development of those regions and the subsequent 30 second BOE of the SOG exposed the gate and doped SOI. Determination of the etch rates of the BOE on the SOG can be found in Appendix B. Although the etched SOG-holes were directly over the desired contacts they were too small to connect electrical wires to. To remedy this large contacts some distance from the MOSFET were required. To create these active region 5 of the photomask was used along with 351 developer to form areas for longer wires with contact pads at their ends. As the SOG was at most 800 nm thick, 900 nm of aluminium was evaporated onto the chips using the electron beam evaporator so as to ensure good coverage. The previously described lift-off process was utilised to remove the excess aluminium. The final step in the cleanroom involved the creation of the back gate. For this, the chip had resist spun onto its front surface and was immersed for 30 seconds in BOE to remove any native oxide on the silicon substrate. The chip was then placed with the silicon substrate facing the evaporant in the e-beam evaporator and at least 200 nm of aluminium evaporated onto this surface.
A.3.5 Final Cleave and Hydrogen Anneal

The chip was cleaved into samples using the diamond scribe and a pair of tweezers. Each sample would be examined under 10x magnification. If the contacts were visually misaligned the sample would be rejected. Those that passed this test were heated to 400 °C in a 99% hydrogen atmosphere for 30 minutes. As described in Chapter 3, this annealing step removed any charged defects or vacancies within the samples that would detrimentally affect the threshold voltages of the gates.

A.3.6 Mounting and Bonding the Samples

The samples were mounted onto chip carriers (figure 4-2(b)) using silver paste. The paste was first painted onto the carrier and the sample gently pushed onto the paste such that the back gate contacted the carrier first. This would then be heated to roughly 120 °C for 40 minutes in order to cure the paste and create an Ohmic contact to the back gate. A wire bonder was used to lay gold wiring between the gold pads around the chip carrier to aluminium contacts on the sample. Once complete, the chip carrier was placed in the sample box (figure 4-2(a)) to be tested.

Figure A-7 shows optical micrographs of finished 2-terminal, 5-terminal, 12-terminal devices and a Corbino disk. All were mounted on chip carriers and their contacts connected to the chip carrier via gold wire wire. The contact pads were 300 µm wide which allowed for a large, easily accessible target when using the wire bonder. The front gate appears as a green region on these devices, although it is only noticeable on the Corbino disk (figure A-7(c)) due to its size.
Figure A-7: Examples of the finished MOSFETs mounted and bonded on chip carriers. Front gate contacts are identified while all other contacts could be used as source-drain connections. These are (a) a 2-terminal, (b) a 5-terminal, (c) a Corbino disk and (d) a 12-terminal.

### A.4 Sample Testing

The samples were initially tested by applying voltages in the range ±50 mV to a given n-type contact while one other contact would be grounded. The voltages were kept small to prevent damage to the device. All other contacts, including the gates, would be left floating to ensure the current flowed only along the contacts under scrutiny. The gates were also checked for current leaks to the SOI layer. If a leak was detected the sample would remain unused. These tests were conducted at room temperature.

It was at this point that problems started to appear as although a current could be passed between the source and drain, all samples leaked current to both gates. Although the source-drain current $I_e$ appeared ohmic over the source-drain voltage range $V_e = ±50$ mV for all samples (figure A-8), the gates would leak if they were grounded or connected to an SMU whilst a source-drain current was flowing. The absolute magnitude of this leak varied with sample and was within the range $I_{\text{leak}} = 0.1 − 5 \mu$A. Keeping the gate connected while floating the drain contact minimally altered the considerable current flowing through the leak.
A.4.1 Potential Causes of the Current Leak

Under 20x magnification a number of potentially detrimental features were observed on the sample surfaces (figure A-9). The first was the cracked SOG potentially leading to pinholes through which any deposited metal could conduct (example in figure A-9(c)). This may have been a source of the short circuit between the front gate and source-drain contacts. Another major problem was the apparent over-etching of the SOG around the top of the front gate. This is identified explicitly on figure A-9(d) but is present on all of the devices. It is entirely possible that the etch rate of the BOE on the SOG was severely underestimated and that in fact the SOI mesa was exposed. Thus, when the aluminum was evaporated, a short circuit would form between the metal contact, polysilicon gate and the SOI layer.
Figure A-9: A number of features are identified on the surface of each sample. Cracks in the SOG and overetched regions around the top of the front gate can be observed. (a) A 2-terminal device. (b) A 5-terminal device. (c) A Corbino disk. (d) A 12-terminal device.

As a result of this failure no measurements of the giant valley splitting at the front SIMOX interface were made. Instead, this chapter continues below with suggestions for future work.
A.5 Suggestions For Improvements

It was thought that the shortcircuits described above arose due to problems with the SOG. It is possible that the cracks in the SOG arose due to the temperature gradient in table A.3 was not low enough and that greater times should have been spent at each step. Using temperatures between those listed in table A.3 would have reduced the overall rate of change of temperature and in doing so reduced any cracking caused by thermal shock. Another major issue was the etch rate of the SOG in the BOE. It would appear that the etch rate was much greater than measured in Appendix B leading to the exposure of the SOI mesa as the SOG was etched isotropically. To remove this problem an etching method that produces an anisotropic profile, such as a reactive ion etch, is recommended for future efforts.

A.6 Conclusions

A serious, time-consuming attempt was made to fabricate SOI MOSFETs using equipment within the University of Bath. Ultimately shortcircuits between the gates and aluminium contacts prevented any measurements at the front SIMOX interface from being performed. It was suggested that the SOG be cured over a greater period of time and with a smaller temperature gradient to minimise any chances of pinholes or cracks developing within its structure. Additionally, an anisotropic etch such as RIE for creating holes through the SOG to the doped regions and front gate should be utilised in future to prevent short circuits between the gate and aluminium contacts.
Appendix B

Etch Rates Determination and the MOSFET Fabrication Process Sheet

In this appendix the determination of the etch rates of the oxide and SOI layers within the Valleytronics wafers described in Appendix A is demonstrated. Also shown is the etch rate of the spin-on-glass used in that chapter. Additionally a process sheet detailing the minutiae of the MOSFET fabrication in Appendix A is presented.

B.1 The Etch Rates

Identifying the etch rates of the different silicon and silicon dioxide layers when immersed respectively in the NAW solution and 5:1 HF was necessary in order to create the MOSFETs in Appendix A. A number of chips from wafers D1 and D2 were used for determining these rates; the results are shown in B-1. Each chip was partially immersed in either the NAW solution (60 ml HNO₃, 3 ml NH₄F and 30 ml de-ionised (DI) H₂O) or 5:1 BOE depending on the layer to be etched. They would be left partially submerged in the etchant for a given time before the depth of removed material was measured using a Dektak Profilometer. Starting with the NAW etch the polysilicon was found to be removed in 30 s. Etch rates for each layer are shown in table B.1. Leaving the chip in the NAW solution for times greater than 30 s leads to etching of the exposed FOX. However, as the etch rate of the NAW on the FOX was low in comparison to the etch rate of the polysilicon it was reasoned that the FOX could be used as an etch stop for the NAW solution. After a rinse with DI water and dry with nitrogen gas to remove any remaining acid the chips would be partially submerged in BOE to etch the FOX. The FOX was removed in 90 s as determined from figure B-1. Leaving the chip in the BOE did not etch the underlying silicon substrate which was used as the etch stop for the BOE. Again, the chips were rinsed with DI water and dried with nitrogen gas to remove any remaining acid. Finally the
silicon substrate was etched with NAW solution. On figure B-1 the two green points at times of 30 and 60 s still had some FOX on the silicon substrate leading to the negligible etching observed. These points were not used when calculating the etch rate of the NAW solution on the silicon substrate. After the FOX had been removed the NAW etched the substrate as can be seen from 90 s onwards in figure B-1.

![Figure B-1: Etch rates for each of the different layers of Wafers D1 and D2. Solid lines are guides while dashed lines delineate the thickness of the polysilicon and front oxide. The silicon substrate was 525 µm thick.](image)

Using the etch rates in table B.1 below and the thicknesses of each layer of the valleytronics wafers used in Appendix A (table A.1) etch times for each layer was calculated. The SOI layer was assumed to possess the same etch rate as the silicon substrate. When performing actual etches a few seconds would be added to the calculated etch time to ensure a completely exposed surface. The method described in Appendix A section A.3.2 was also used to further ensure all required material was removed.

<table>
<thead>
<tr>
<th>Layer and etchant</th>
<th>Etch rate (nm/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polysilicon (NAW solution)</td>
<td>3.05</td>
</tr>
<tr>
<td>FOX (BOE)</td>
<td>0.83</td>
</tr>
<tr>
<td>Silicon substrate (NAW solution)</td>
<td>2.33</td>
</tr>
</tbody>
</table>

Table B.1: The etch rates of the NAW and BOE on the polysilicon, FOX and silicon substrates of wafers D1 and D2.

To determine the etch rate of the spin-on-glass some was spun onto unused chips cleaved from wafers D1 and D2 as detailed in Appendix A. After following the curing regime in Appendix A (table A.3) the chips were partially submerged in the same BOE solution as was used for the
previously described FOX etch. The results in figure B-2 do not provide a definitive etch rate for the SOG however, at its thickest the SOG required no more than 30 s to be etched away completely. From this it was concluded that when making the actual MOSFETs they should be immersed for no longer than 30s to ensure that the SOG was removed in the desired locations while minimising any overetching of the SOG.

![Graph showing etch rates for spin-on-glass.](image)

Figure B-2: Etch rates for the spin-on-glass. The solid lines are guides to the eye.

## B.2 Fabrication Process Sheet

The table below shows every step in the fabrication process. For each step a description and some notes that give a short explanation as to why that step was executed are detailed. Some processes were repeated and so are only described in full once. It is important to note that the time between an HF etch and the SOI doping or aluminium evaporation was no longer than two hours so as to prevent a native oxide forming on the bare silicon.

<table>
<thead>
<tr>
<th>Process Name</th>
<th>Description</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer cleaving</td>
<td>A diamond scribe and tweezers were used to cleave the wafer into roughly cm²</td>
<td>Each photomask is a cm² in area.</td>
</tr>
<tr>
<td>Piranha clean</td>
<td>Wafers immersed in a Piranha solution - 40 ml H₂O₂ and H₂SO₄ - for 10 minutes. A 5 minute rinse in de-ionised (DI) H₂O follows.</td>
<td>The Piranha removed any organic detritus on the wafer. The rinse removes any remaining piranha solution.</td>
</tr>
<tr>
<td>Process</td>
<td>Details</td>
<td></td>
</tr>
<tr>
<td>--------------------------------</td>
<td>------------------------------------------------------------------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>Photoresist spin</td>
<td>S1813 photoresist was spun onto the surface of the wafers using a resist spinner. The spin speed was initially 500 rpm for 5 s followed by 3000 rpm for 30 s. The resist acts as a mask for later processes. The spin speeds produce a uniform surface that is of sufficient thickness to withstand later development steps.</td>
<td></td>
</tr>
<tr>
<td>Post-bake</td>
<td>The resist covered wafers were left in a 90° C oven for 1 hour. The heating cures the resist.</td>
<td></td>
</tr>
<tr>
<td>Edge bead removal</td>
<td>Use of the mask aligner to expose the edges of the wafer to UV light for 10 s. A solution of 70 ml of DI H₂O to 20 ml 351 developer (351 solution) was used to develop the exposed photoresist until the edge beads were no more. A 5 minute post-bake at 90° C follows. Removing the edge beads improves alignment between the photomask and the wafer. The 5 minute post-bake evaporates any remaining 351 solvent.</td>
<td></td>
</tr>
<tr>
<td>Mesa formation</td>
<td>Active area 1 was used in conjunction with the mask aligner to expose the photoresist for 5 s to UV radiation. A 351 solution was used to develop the exposed photoresist for 30 to 40 s. A 30 minute post-bake at 90° C follows (30 min post-bake). This mask forms the outline of what would become the mesa. Heating hardened the resist against etching in the next steps.</td>
<td></td>
</tr>
<tr>
<td>Nitric acid (NAW) etch</td>
<td>Chips immersed in a solution of 60 ml HNO₃, 3 ml NH₄F and 30 ml DI H₂O (NAW solution) for 60 s. A 30 s rinse in DI H₂O follows. This etch removes the exposed polysilicon.</td>
<td></td>
</tr>
<tr>
<td>5:1 buffered oxide etch (BOE)</td>
<td>Chips immersed in 5:1 BOE for 260 s. A 30 s rinse in DI H₂O followed (BOE immersion). This etch removes the FOX. The etch length depended on the oxide thickness of the chip.</td>
<td></td>
</tr>
<tr>
<td>NAW etch</td>
<td>Chips immersed in NAW solution. A 30 s rinse in DI H₂O follows. This etch finished the mesa formation by removing the SOI. The etch time was dependent on the thickness of the silicon.</td>
<td></td>
</tr>
<tr>
<td>Photoresist spin</td>
<td>Resist spin</td>
<td></td>
</tr>
<tr>
<td>Post-bake</td>
<td>1 hour bake</td>
<td></td>
</tr>
<tr>
<td>Edge bead removal</td>
<td>See previous edge bead removal</td>
<td></td>
</tr>
<tr>
<td>Step</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>------</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>Gate definition</td>
<td>Active area 2 is used to expose the resist covered chips for 5 s to UV. Developed and baked for 5 minutes as above. The resist here covers what will become the front gate.</td>
<td></td>
</tr>
<tr>
<td>NAW etch and photoresist removal</td>
<td>Wafers immersed NAW solution. A 30 s rinse in DI H$_2$O follows. The photoresist is removed by immersion in acetone and IPA. Here the polysilicon front gate is formed and the front oxide exposed. The remaining resist was removed with acetone.</td>
<td></td>
</tr>
<tr>
<td>Photoresist spin</td>
<td>Resist spin</td>
<td></td>
</tr>
<tr>
<td>Post-bake</td>
<td>1 hour bake</td>
<td></td>
</tr>
<tr>
<td>Edge bead removal</td>
<td>See previous edge bead removal</td>
<td></td>
</tr>
<tr>
<td>SOI exposure</td>
<td>Active area 3, the mask aligner and 351 solution are used to remove resist. FOX above the SOI is exposed for etching in the next step.</td>
<td></td>
</tr>
<tr>
<td>5:1 BOE</td>
<td>BOE immersion Here the FOX is etched and the SOI was exposed for doping.</td>
<td></td>
</tr>
<tr>
<td>Thermal/electron beam evaporation of AuSb</td>
<td>80 nm of AuSb was evaporated onto the wafer using a thermal evaporator. The AuSb is an n-type dopant.</td>
<td></td>
</tr>
<tr>
<td>Lift-off of photoresist (Lift-off)</td>
<td>The wafer was immersed in acetone and subjected to ultrasound (Lift-off) The acetone removes resist while the ultrasound agitates and removes any loose material.</td>
<td></td>
</tr>
<tr>
<td>Spin-on-glass (SOG) deposition and curing</td>
<td>SOG was pipetted onto the chip surface and spun using the ‘resist spin’ recipe. This was immediately followed by heating at 74, 150, 200 and 300° C each for 10 minutes. The chip was finally cured at 400 °C for 1 hr in ambient atmosphere. The SOG acts as an insulating layer. This curing process minimised the appearance of cracks in the SOG while the high temperature used acted as the drive-in for the dopant material.</td>
<td></td>
</tr>
<tr>
<td>Photoresist spin</td>
<td>Resist spin</td>
<td></td>
</tr>
<tr>
<td>Post-bake</td>
<td>1 hour bake</td>
<td></td>
</tr>
<tr>
<td>Edge bead removal</td>
<td>See previous edge bead removal</td>
<td></td>
</tr>
<tr>
<td>SOG hole preparation</td>
<td>Active region 4, the mask aligner and 351 solution were used to remove resist. The developed resist revealed SOG directly above the front gate and the doped regions of SOI.</td>
<td></td>
</tr>
<tr>
<td>SOG etch</td>
<td>BOE immersion for 30 s. This etched the exposed SOG down to the doped SOI.</td>
<td></td>
</tr>
</tbody>
</table>
Electron beam evaporation of Al

At least 900 nm of Al was evaporated onto the front surface of the chip.
The Al on the SOG formed the contacts to the gate and n-type silicon.

<table>
<thead>
<tr>
<th>Lift-off</th>
<th>Lift-off process</th>
</tr>
</thead>
<tbody>
<tr>
<td>Photoresist spin</td>
<td>Resist spin</td>
</tr>
<tr>
<td>Post-bake</td>
<td>1 hour bake</td>
</tr>
<tr>
<td>5:1 BOE</td>
<td>BOE immersion</td>
</tr>
<tr>
<td>Electron beam evaporation of Al</td>
<td>At least 200 nm of Al was evaporated onto the back surface of the chip.</td>
</tr>
<tr>
<td>Passivation</td>
<td>A mixture of 95% H₂ and 5% N₂ gases were flowed over the chip.</td>
</tr>
<tr>
<td>Final cleaving</td>
<td>A diamond scribe and tweezers were used to cleave the chip into as many samples as are present</td>
</tr>
<tr>
<td></td>
<td>The native oxide on the backside of the chip was removed here.</td>
</tr>
<tr>
<td></td>
<td>This formed the back gate.</td>
</tr>
<tr>
<td></td>
<td>The hydrogen eliminated dangling bonds in the chip’s structure.</td>
</tr>
<tr>
<td></td>
<td>The cleaved samples would then be used in later experiments.</td>
</tr>
</tbody>
</table>
Appendix C

The LabVIEW Program

This appendix provides an overview of the LabVIEW program used to acquire data during experiments. Schematic diagrams of the code are shown and the

C.1 LabVIEW Introduction

As discussed in Chapter 4 LabVIEW was used because a single program allows for the communication of a number of different SMUs all from different suppliers. Although each SMU required its own software drivers for use in LabVIEW these were readily obtained from the supplier’s website. Data from the SMUs were then be compiled into a file that was readable by the Origin 8.5 software used to analyse data.

Any LabVIEW program is composed of two, on-screen windows; the block diagram and the front panel. The block diagram is where 'code' is written. Commands, functions and SMU drivers were placed here and connected, or wired, together. The inputs for the commands, functions and SMUs appear on the front panel. It is on this panel that the experimentalist enters values to be used by the program.

C.2 The Program

A schematic diagram of the program is shown in figure C-1. It allowed for the use of up to three Keithley SMUs, the Agilent SMU and the lock-in amplifiers. Wait commands were implemented within the code to ensure that all the SMUs waited for a user-set time between applying some voltage and measuring a current. This ensured that there was no lag between the devices when obtaining data. As it was not always necessary to use them, the lock-ins could be ignored by the code at the users discretion by pressing the relevant button on the front panel. It was also on the front panel that the user decided the number of SMUs to use. It was here that initial and final voltages were input into the program to be applied by the relevant SMUs. The user could also decide whether to set each SMU to a constant value, continuous sweep or some discrete steps between the set values. This was important as in a
A typical experiment required a constant source-drain voltage, continuously swept front gate voltage and discretely changing back gate voltage were all required simultaneously. For especially long runs, the program would be left running over a weekend. A given SMU applying a voltage would also measure the relevant current. As an example, the SMU applying the source-drain voltage would also measure the source-drain current. Once the experimentalist had set the program up with the required inputs and ranges, the program would send the relevant starting voltages to each SMU. This would cause the program to ramp up the voltages on the sample at a rate of ±1 V per second dependent upon the sign of the initial value. During the program’s operation, applied voltages and measured currents were saved in a file created by the program (figure (C-1)(e)). Once all the final parameters had been reached, the program would slowly reduce the voltages to 0 V (C-1)(f)). Sometimes it was necessary to stop the program in the middle of an experimental run. The preferred way of doing this was to press the user-built stop button in the front panel as that would gently ramp all applied values to zero before ending the program. The other method was to use the inbuilt terminate button built into LabVIEW. This would cease communication between the computer and the SMUs, stopping them at whatever voltage they were applying to the sample at that particular time. This could potentially damage the sample, especially if large voltages were in use. This method was used rarely and only as a last resort.

Figure C-1: A schematic of the block diagram in Labview (a) User-entered data such as number of Keithleys to use, use of the lock-in amplifiers, type of sweep, are checked and in (b) the sanity checks are performed. If the sanity checks fail an error message is displayed informing the user of what needs correcting before the program can run. (c) If the user required the lock-in amplifiers to be used this part of the block diagram activates. If not, then this section remains inactive. (d) The drivers for the Keithley SMUs appear here. Voltages are sent to the SMUs and source-drain currents measured. Data they obtain is passed to (e) where a file containing this information is created. (f) Once the program has finished, this section is entered and all voltages are set to zero; the program then stops. This section can also be entered if the user presses the stop button on the front panel.

C.2.1 Safety and Sanity Checks

To ensure samples were not damaged inadvertently and that experiments were run efficiently, the following code was added to the program. To prevent sample destruction maximum gate...
voltages of $V_F = \pm 16$ V, $V_B = \pm 60$ V and $V_{e,h} = \pm 1.5$ V were set. Attempts by the user to apply voltages greater than these values resulted in an error message informing the user that one or more voltage values were too large. The program would not run in this instance. Additionally, when deciding how many SMUs to use and whether they should be set to constant, continuous or discrete there were certain combinations of these that were useless for obtaining data. For example, simultaneously sweeping the source-drain voltage and both gate voltages while measuring the source-drain current would result in non-nonsensical data. This could potentially waste experimental time which was critical when liquid helium was being used. To prevent errors like this occurring a section of code was added to ensure that the combination set by the experimentalist was sensible. If it were not, an error message would be displayed informing the user that at least one of the SMUs settings, specifically the continuous, constant or discrete settings, needed altering in order for the program to run. The program would not run in this instance.
Bibliography


[18] Junsaku Nitta, Tatsushi Akazaki, Hideaki Takayanagi, and Takatomo Enoki. Gate control of spin-orbit interaction in an inverted In$_{0.53}$Ga$_{0.47}$As/In$_{0.52}$AlAs heterostructure. *Physical Review Letters, 78*:1335 to 1338, Feb 1997.


[118] Keithley. *Series 2400: SourceMeter*® *SMU Instruments*.


[134] Kei Takashina. Data from 15 T magneto-resistance experiment utilising a 2DHG in a Si/SiO$_2$ based MOSFET.


