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Optimal geometric aspect ratio of thin film transistors for low-cost flexible CMOS inverters

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A low-cost, flexible processor is essential to realise affordable flexible electronic systems and transform everyday objects into smart-objects. Thin film transistors (TFTs) based on metal-oxides (or organics) are ideal candidates as they can be manufactured at low processing temperatures and low-cost per unit area, unlike traditional silicon devices. The development of complementary metal-oxide-semiconductor (CMOS) technology based on these materials remains challenging due to differences in performance between n- and p-type TFTs. Typically the width-to-length ratio (*W/L*) of the lower mobility p-type TFT (n-type for organics, referred to in brackets from here onwards), is scaled up inversely with mobility to match the higher on-current of the n-type (p-type) TFT; this is also common for silicon CMOS technology. However, this method is unsuitable for transistors where not only the on-current but also the off-current scales with *W/L*, including flexible p-type metal-oxide and n-type organic TFTs. Here we propose the concept of an optimal geometric aspect ratio that can be applied universally to silicon, metal-oxide and organic complementary inverters. This ratio determines the *W/L* of the p-type (n-type) transistor that maximises the inverter efficiency represented by the average switching current divided by the static currents. Notably, our results show that reducing *W/L* of metal-oxide p-type TFTs increases the inverter efficiency while reducing the area compared to simply scaling up *W/L* inversely with mobility. A high inverter efficiency is critical to reduce static power consumption and increase the gate density of flexible processors. We anticipate this work provides a straightforward method to geometrically optimise flexible CMOS inverters which will remain relevant even as the performance of TFTs continues to evolve.

Index terms – complementary metal-oxide semiconductor (CMOS), inverter, indium-silicon-oxide (ISO), metal-oxide, tin monoxide (SnO), thin film transistor (TFT), organic, off-current, geometric aspect ratio

Introduction

Flexible electronic devices are fabricated on substrates such as paper, polymer and metal foil [1]. Metal-oxides, organics and amorphous silicon are commonly used active materials. Compared to traditional silicon devices, they offer a number of advantages including thinness, conformability and low manufacturing costs. Mature low-cost, thin, flexible and conformable devices have been succesfully developed. These include sensors [2], memories [3], batteries [4], light-emitting diodes, energy harvesters [5], near-field communication/radio frequency identification [6] and printed circuitry such as antennas; essential electronic components to build any smart integrated electronic device. A low-cost flexible microprocessor employing CMOS technology is yet to be realised. Silicon processors are unsuitable as they are unlikely to reach a price point at which everyday items, such as bottles, food packaging, and wearables, can be turned into smart-objects. Therefore, there is a strong interest in low-power circuit designs and larger-scale integration of flexible thin film transistors (TFTs). Processors have been fabricated using low-temperature poly-silicon (LTPS) TFTs [7] but high manufacturing costs and poor scalability of this technique make it unsuitable for high-volume, low-cost, flexible integrated smart systems [8]. Organics are also actively researched and excellent low-voltage CMOS inverters have been reported [9]–[11]. However, their use is limited to low-end backplane and circuit applications due to lower mobility, stability, uniformity and limited scalability [8]. Metal-oxides are arguably the most promising due to their high mobility, excellent spatial uniformity and scalability. A flexible

processing engine fabricated with 0.8-µm n-type metal-oxide TFT technology has recently been reported [12]. It contains ~1,000 gates (resistive load logic) and its gate-density is 45 times higher than previous metal-oxide processors [3], [12]–[15]. The same authors have since fabricated a flexible 32-bit processor consisting of 18,334 gates [14]. Earlier this year, the same TFT technology was used to fabricate a flexible microprocessor using pseudo-CMOS logic [16]. While these works show the potential of metal-oxide processors, they also highlight its main shortcoming; only n-type TFTs were used since there is currently considered to be no compatible p-type material. Any further increase in gates requires CMOS technology as the static power consumption, P_{stat}, of unipolar technology becomes unfeasibly high [14][16].

CMOS technology, which combines n- and p-type TFTs, benefits from low power consumption, high circuit integration density, high logic output, and high noise margins [17]. The development of thin film CMOS is therefore vital for low-cost flexible processors. Ideally, the output characteristics of n- and p-type TFTs in complementary inverters are perfectly matched. Indeed, the success of silicon CMOS is partly due to excellent control of n- and p-type MOSFET characteristics. In contrast the use of oxides and organics is challenging due to poor performance of oxide p-type and n-type organic TFTs relative to silicon MOSFETs.

Development of p-type oxide TFTs has been hampered by the low mobility and current-switching-ratio (I_{on}/I_{off}) caused by the high off-state current, I_{off}, that is typically observed [18][19]. Cuprous oxide (Cu_2O) and tin monoxide (SnO) TFTs demonstrate promising results but mobilities are generally limited to ~ 1 cm^2/Vs [19][20]. Both these materials, but primarily SnO, have been used in all-oxide CMOS inverters [20][21]. A high geometric aspect ratio, $(W/L)_p/(W/L)_n$, is normally used to increase the maximum output current, I_{max}, of the p-type TFT to match the n-type TFT using the same design rule that is applied to silicon CMOS.

For silicon CMOS this method results in an excellent match of the n- and p-type output characteristics provided the threshold voltages (V_{th}) of the n- and p-type transistor are approximately equal and opposite in sign (ideally close to 0V). Moreover, the transistors should fit the standard MOSFET equations well with a constant saturation mobility. As a result the propagation delays of the low-to-high and high-to-low transitions are roughly equal and the switching voltage is approximately $V_{DD}/2$, maximising noise margins. In the Supplementary Information, the static states of the CMOS inverter and dynamic low-to-high and high-to-low transitions are illustrated, along with the terminology for the different performance variables used in this work. Ideally, both the n- and p-type transistors exhibit complete channel depletion in the off-state and have a turn-on voltage, V_{on}, of ~ 0V. In this case, the minimum output current at V_{GS} = 0V, I_{min}, and I_{off} both remain constant as the width-to-length ratio (W/L) (or V_{DS}) is increased. Since I_{stat} of the p-type device equals I_{min}, increasing $(W/L)_p$ (or V_{DS}) does not affect P_{stat} of the inverter. This represents the ideal ('silicon') scenario (Fig. 1a,b,f,g). Note there are subthreshold models for Si transistors showing the off-current roughly scales with W/L and therefore P_{stat} of the inverter does increase with W/L [22]. However, for Si CMOS inverters the effect is negligible as the overall power consumption is dominated by the dynamic power (due to the higher operation frequency and low off-current).

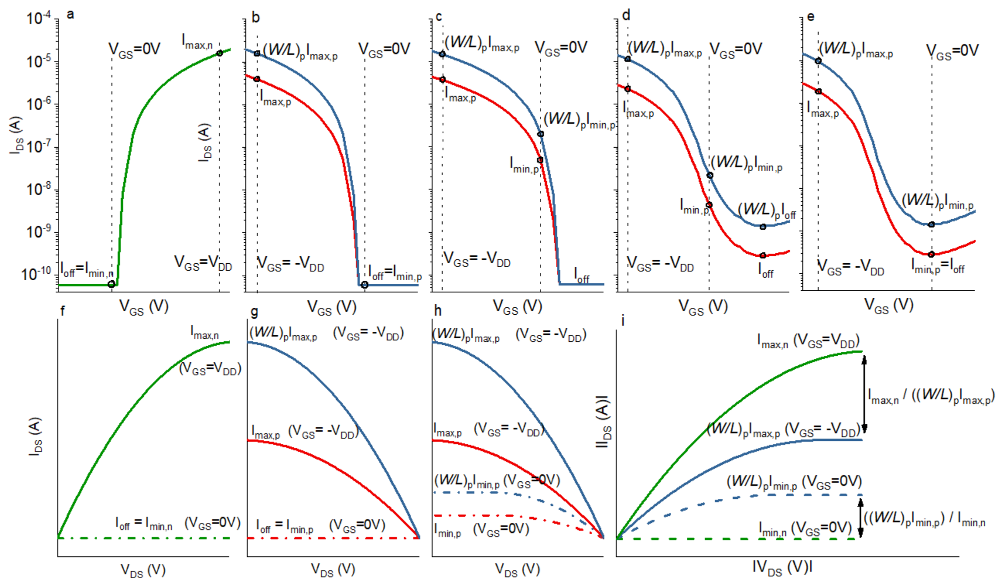

Fig. 1. Transfer characteristics and output characteristics of: (a,f) 'ideal silicon' n-type transistor with V_{on} ~0V and complete channel depletion; I_{off}=$I_{min,n}$ does not scale with $(W/L)_n$. (b,g) p-type transistor with V_{on} ~0V and complete channel depletion; to match the higher mobility of the n-type, $I_{max,p}$ is scaled by $(W/L)_p$, I_{off}=$I_{min,p}$ does not scale with $(W/L)_p$. (c,h) p-type transistor with V_{on} >0V and complete channel depletion; at V_{GS}=0V the transistor is partly turned on and both $I_{max,p}$ and $I_{min,p}$ scale with $(W/L)_p$. (d,e,h) 'oxide' p-type transistor without complete channel depletion; both I_{off} and $I_{min,p}$ scale with $(W/L)_p$. (i) Maximum and minimum output currents for n- (green) and p-type transistors, and the ratio between them after scaling with $(W/L)_p$.

Simply scaling *W/L* inversely with mobility does not work well for (flexible) TFTs based on metal-oxides and organics as large differences (in mobility, subthreshold swing, I_{on}, I_{off}, V_{th}) remain between the performance of n- and p-type TFTs. It is therefore surprising to see that this method is widely used for TFT-based CMOS inverters. As reported for Cu_2O [18], we observe in SnO that I_{off} scales with V_{DS} and $(W/L)_p$. This dependence is likely due to accumulation of electrons in the off-state, which decreases channel resistance [18]. This suggests a common mechanism for p-type oxides. Therefore, increasing $(W/L)_p$ also increases I_{off} and I_{min} (Fig. 1d,e,h). Considering I_{off} of metal-oxide p-type TFTs is typically at least 10-fold higher than for its n-type counterpart, simply scaling up $(W/L)_p$ so that $I_{max,n} = (W/L)_p I_{max,p}$ creates an even greater mismatch between the off-currents and directly increases P_{stat} of the inverter. A similar effect can be observed for p-type (n-type for organics case, referred to in brackets from here onwards) transistors where V_{on} is considerably above (below) 0V. The transistor is now partly turned on at V_{GS} = 0V and I_{min} also scales with V_{DS} and *W/L* (Fig. 1c,h). This can be observed in many transistors, including n-type organic and p-type oxide TFTs, where precise control of characteristics remains challenging. The dependence of I_{min} on *W/L* is likely to remain an issue even as the performance of TFTs improves. Moreover new transistor technologies may emerge in the future with similar characteristics.

In this work, we experimentally investigate the effects of changing *W/L* of a p-type SnO TFT on the voltage transfer characteristics (VTC) and current transfer characteristics (CTC) of all-oxide CMOS inverters. We fabricated n-type amorphous indium-silicon-oxide (a-ISO) TFTs and p-type SnO TFTs to combine them into all-oxide CMOS inverters. A model was developed to verify CMOS performance and compare it to the ideally matched case, as well as a unipolar resistive load inverter. We define inverter efficiency, I_p/I_{stat}, as the average switching current (I_p) divided by the sum of the static currents (I_{stat}). We show that reducing *W/L* of metal-oxide p-type TFTs increases I_p/I_{stat} compared to simply scaling up *W/L* inversely with mobility, while reducing the area.

Finally, we propose the concept of an optimal geometric aspect ratio which is universally applicable to silicon, metal-oxide and organic complementary inverters. This ratio determines the *W/L* of the p-type (n-type) transistor that best matches the maximum and minimum output currents of both n- and p-type TFTs equally so that inverter efficiency is maximised. This is critical to reduce the static power consumption (P_{stat}) and enable large-scale integration of metal-oxide TFTs. We estimate that by using the approach developed in this work it is possible to reduce P_{stat} by a factor > 100 and increase I_p/I_{stat} by a factor > 100, compared to unipolar resistive technology, based on the current performance of p-type SnO TFTs, thus enabling a further increase in gate density.

Characteristics of n-type a-ISO and p-type SnO TFTs

Fig. 2d,i show schematics of the a-ISO and SnO TFTs (fabrication details provided in Methods). The a-ISO TFT (*W/L* = 20) has an ideal V_{on} of ~0V and I_{off} of ~400 pA as shown in Fig. 2a. I_{off} is independent of V_{DS} which demonstrates

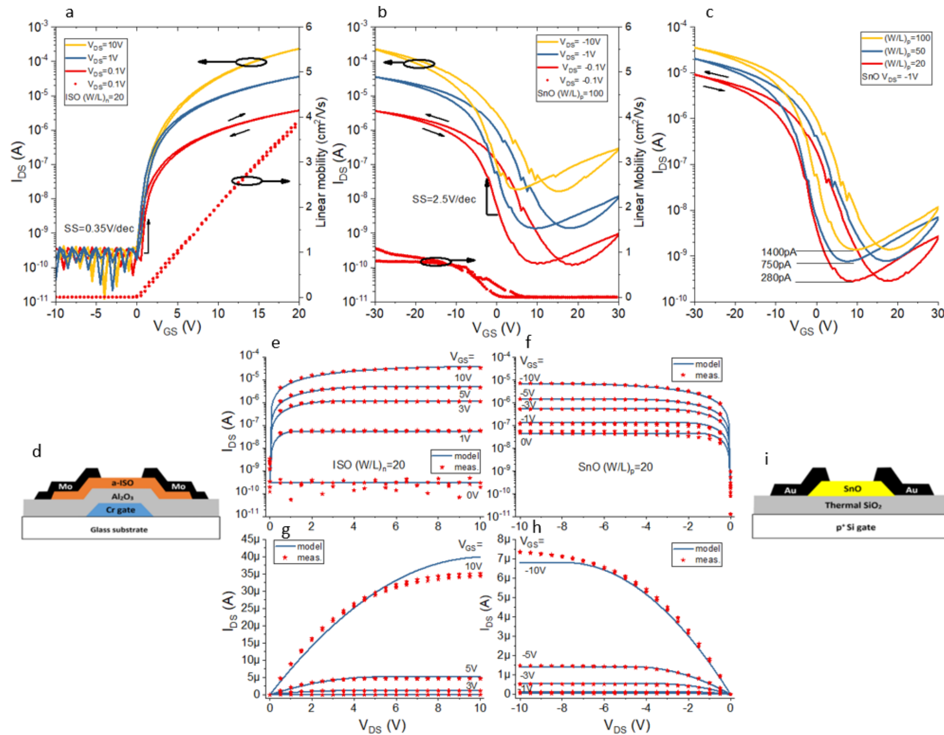

Fig. 2. Experimentally measured transfer characteristics and linear mobility of (a) a-ISO TFT and (b) SnO TFT. Transfer characteristics of SnO TFT with different *W/L* ratios (c). Output characteristics (red) and modelled curves (blue) of the a-ISO TFT and the SnO TFT (b,d) in log (e,f) and linear scales (g,h). Schematic cross section of (d) the a-ISO TFT and (i) SnO TFT

complete channel depletion. The subthreshold swing (*SS*) is 0.35 V/dec, the I_{on}/I_{off} is ~10^6 for $V_{DS} = 10$ V, and the threshold voltage (V_{th}) is 0.2V. The mobility increases linearly and reaches 4cm^2/Vs at $V_{GS} = 20$ V. For the SnO TFT (Fig. 2b,c), V_{on} is ~8 V and I_{off} ranges from 200 pA to 20 nA as V_{DS} varies from -0.1 V to -10 V (for $W/L = 100$) indicating the difficulty to turn off the device. This scaling of I_{off} with V_{DS} and W/L is commonly observed for p-type oxides like SnO and Cu_2O [18], [23]–[26]. The SnO transfer characteristics in Fig. 2c exhibit similar dependence; for W/L ratios of 20, 50 and 100, I_{off} is 280, 750 and 1400 pA respectively. The parameters of the SnO TFT are as follows; SS = 2.5V/dec, the I_{on}/I_{off} is ~2×10^4 for $V_{GS} = [-10$ V, 30 V$]$, and $V_{th} = 2.3$ V. The mobility increases linearly up to $V_{GS} = -10$ V and then saturates at ~1 cm^2/Vs, as shown in Fig. 2b. Hysteresis is a common problem for SnO TFTs and is likely caused by the high trap state density near the interface between the SnO layer and the SiO_2 insulator. It has been shown that (alumina) interfacial layers can help to reduce the high trap state density [27].

The output characteristics of both TFTs exhibit a clear linear and saturation region as shown in Fig. 2g,h ($W/L = 20$ for both TFTs). The saturation current of the a-ISO TFT ranges from $I_{min,n} = 300$ pA ($V_{GS} = 0$V) to $I_{max,n} = 35$ µA ($V_{GS} = 10$ V). The range of the SnO TFT ($(W/L)_p = 20$) is smaller and varies from $I_{min,p} = 60$ nA to $I_{max,p} = 7$ µA. In a CMOS inverter, the output characteristics of the n- and p-type transistors are ideally matched exactly, and usually $(W/L)_p$ is increased to match the higher mobility and on-current of the n-type device. This can be achieved by setting $(W/L)_p = 100$. In this case the output currents align more closely for $V_{GS} = [3,5,10$V$]$ but the gap increases for $V_{GS} = [0,1$V$]$ since I_{off} of the p-type device scales with $(W/L)_p$. This raises the question whether increasing $(W/L)_p$ actually improves the inverter performance.

Modelling of inverters

A model for the output characteristics was developed based on the standard MOSFET equations modified by a pre-factor, $\alpha(V_{GS} - V_{th,n})$, where $V_{th,n}$ is the threshold of the n-type TFT. This takes into account the linear dependence of mobility on V_{GS}, as shown in Fig. 2a,b. The equations for the a-ISO and SnO TFTs in the linear regime respectively are:

$$I_{DS,n} = \left(\frac{W}{L}\right)_n C_{ox,n}\alpha(V_{GS} - V_{th,n})\left((V_{GS} - V_{th,n})V_{DS} - \beta {V_{DS}}^2\right) + I_{OFF,n} \quad (1)$$

$$I_{DS,p} = \left(\frac{W}{L}\right)_p (C_{ox,p}\gamma(V_{GS} - V_{th,p})\left((V_{GS} - V_{th,p})V_{DS} - \delta {V_{DS}}^2\right) + I_{OFF,p}) \quad (2)$$

In the saturation regime $I_{DS,n}$ and $I_{DS,p}$ equal the maximum value when $\frac{\partial I_{DS}}{\partial V_{DS}} = 0$ (further details in Supplementary Information). Fig. 2e,f,g,h show the model closely fits the measured data. The logarithmic graphs in Fig. 2e,f show a

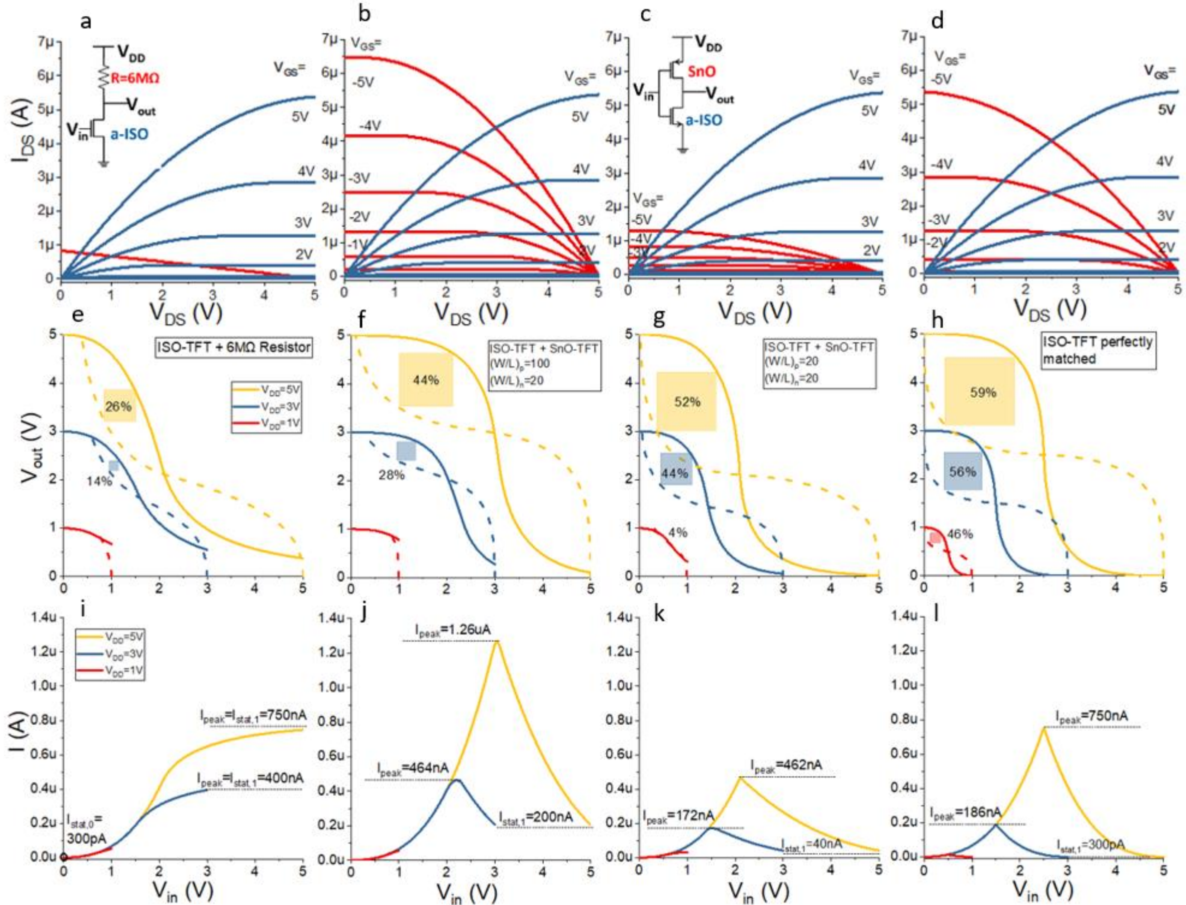

Fig. 3. Output characteristics of ISO TFT $(W/L)_n$=20 (blue) with (a) 6MΩ resistor, (b) SnO $(W/L)_p$=100, (c) SnO $(W/L)_p$=20, (d) perfectly matched p-type TFT. (e, f, g, h) Corresponding inverter voltage transfer characteristics, MEC noise margins are represented by the largest square between the transfer curves. (i, j, k, l) Inverter current transfer characteristics.

good match for lower V_{GS} and especially for I_{min}, which represents the static off-current of the CMOS inverter when $V_{in} = V_{GS}$ is low (0V) and high (V_{DD}) for the n- and p-type devices, respectively. Fig. 2g,h demonstrate a good fit on a linear scale at higher V_{GS}. We created a MATLAB model of an inverter in which the n-type a-ISO TFT functions as the pull-down network with a range of different loads. The model simulates the VTC and CTC based on the intersection points of the output characteristics. Fig. 3 shows the simulation results of four different configurations.

The configuration in Fig. 3a,e,i contains a 6 MΩ load and is similar to unipolar resistive inverters currently used in several flexible processors [12]–[14]. The VTC show a limited output swing since $V_{out} > 0.5$V. The Maximum Equal Criteria (MEC) noise margin (NM) is 26% of the maximum value of $V_{DD}/2$ for V_{DD} = 5V. The output swing and NMs decline drastically as V_{DD} is reduced to 3V and 1V. The CTC shows the static current at V_{in} = 0V ($I_{stat,0}$) is negligible ($I_{stat,0} = I_{min,n}$ = 300 pA). The resistor current increases, reaching its peak (I_{peak}) when $V_{in} = V_{DD}$. Therefore, the static current at $V_{in} = V_{DD}$ ($I_{stat,1}$) is 400 nA and 750 nA for V_{DD} = 3V and V_{DD} = 5V respectively, which is >1000-fold greater than $I_{stat,0}$.

In Fig. 3d,h,l the resistor is replaced with a theoretically ideal p-type TFT with the same output characteristics as the n-type a-ISO TFT to form a complementary inverter. This represents an ideal setup for comparison as metal-oxide p-type TFTs with this performance do not currently exist. The CMOS inverter characteristics are excellent; even at V_{DD} = 1V it achieves a rail-to-rail swing and NM = 46%. Most importantly the p-type TFT turns off when $V_{in} = V_{DD}$, meaning $I_{stat,1} = I_{min,p}$ = 400 pA. I_{peak} is still ~750 nA when $V_{in} = V_{DD}/2$ but both of the static currents are only 400pA, reducing P_{stat} by >1000-fold. This advantage of CMOS operation is essential for high-density circuits.

VTCs, NMs and gain are widely reported for inverters but provide little information about switching speed and (static) power consumption (i.e. from this information alone it is impossible to tell whether an inverter is an 'efficient' CMOS inverter or a resistive load inverter). Here we define a dimensionless inverter efficiency, I_p/I_{stat}, as the average switching current divided by the sum of the static currents, ($I_{stat}= I_{stat,0}+I_{stat,1}$). The average switching current, I_p, is defined such that it scales with the switching frequency (f). f scales with the inverse of the overall propagation delay (t_p), where t_p equals the sum of the high-to-low (t_{pHL}) and low-to-high (t_{pLH}) transitions. For constant V_{DD}, the time taken to discharge and charge a constant load capacitance (C_L) scales with the inverse of the maximum discharge ($I_{max,HL}$) and charge current ($I_{max,LH}$) respectively (see equation (3)). Therefore, f scales with $I_{max,HL}I_{max,LH}/(I_{max,HL}+I_{max,LH})$ which we define as I_p.

$$f \propto \frac{1}{t_p} = \frac{1}{t_{pHL}+t_{pLH}} \propto \frac{1}{\frac{C_L V_{DD}}{I_{max,HL}}+\frac{C_L V_{DD}}{I_{max,LH}}} \propto \frac{I_{max,HL}I_{max,LH}}{I_{max,HL}+I_{max,LH}} = I_p \quad (3)$$

Note in reality the shape of $I_{max,HL}$ and $I_{max,LH}$ (as a function of the voltage across C_L) also affects t_{pHL} and t_{pLH} but we ignore this as a second order effect. This leads to the dimensionless definition for the inverter efficiency in equation (4). This is an excellent performance parameter as it leverages switching speed over static power and provides a way to quantify this.

$$inverter\ efficiency: \frac{I_p}{I_{stat}} = \frac{\frac{I_{max,HL}I_{max,LH}}{I_{max,HL}+I_{max,LH}}}{I_{stat,0}+I_{stat,1}} \quad (4)$$

For the basic n-type unipolar resistive load inverter $I_{max,HL}$= $I_{max,n}$, $I_{stat,0}$=$I_{min,n}$, and $I_{max,LH}$=$I_{stat,1}$=$I_{max,R}$ where $I_{max,R}$ is the peak current through the resistor. This results in an upper bound of $I_p/I_{stat} < 1$ (equation (5)) since $I_{min,n}$ is generally negligible compared to $I_{max,R}$ and represents a 'worst-case scenario'. For the inverter in Fig. 3a,e,i I_p/I_{stat}=0.86.

$$n-type\ resistive\ load: \frac{I_p}{I_{stat}} = \frac{\frac{I_{max,n}I_{max,R}}{I_{max,n}+I_{max,R}}}{I_{min,n}+I_{max,R}} \approx \frac{I_{max,n}}{I_{max,n}+I_{max,R}} < 1 \quad (5)$$

For the CMOS inverter, $I_{max,HL} = I_{max,n}$, $I_{max,LH} = I_{max,p}$, $I_{stat,0} = I_{min,n}$, and $I_{stat,1} = I_{min,p}$. This results in the inverter efficiency in equation (6). I_p/I_{stat} for the perfectly matched CMOS is given in equation (7) using $I_{max,n} = I_{max,p} = I_{max}$ and $I_{min,n} = I_{min,p} = I_{min}$.

$$CMOS: \frac{I_p}{I_{stat}} = \frac{\frac{I_{max,n}I_{max,p}}{I_{max,n}+I_{max,p}}}{I_{min,n}+I_{min,p}} \quad (6)$$

$$perfectly\ matched\ CMOS: \frac{I_p}{I_{stat}} = \frac{\frac{I_{max}I_{max}}{I_{max}+I_{max}}}{I_{min}+I_{min}} = \frac{0.5I_{max}}{2I_{min}} = \frac{I_{max}}{4I_{min}} \propto \frac{I_{max}}{I_{min}} \quad (7)$$

For the perfectly matched inverter in Fig. 3d,h,l, $I_p=0.5I_{max,n}$= 2.7 µA, $I_{stat}=2I_{min,n}$=800pA, I_p/I_{stat}=3300 (at V_{DD} = 5V). The performance of the SnO TFTs is inferior to that of the a-ISO TFTs and therefore I_p/I_{stat} should be somewhere between 1 and 3300 for an a-ISO/SnO CMOS inverter.

In Fig. 3b,f,j the resistor has been replaced with the p-type SnO TFT with $(W/L)_p$ = 100 to form a complementary inverter with $(W/L)_p/(W/L)_n$ = 5. Increasing $(W/L)_p/(W/L)_n$ is common practice [21], [28], [29] to compensate for the lower mobility of the p-type TFT. In this case, the output currents are matched at V_{GS}=5V but the mismatch at V_{GS} = 0V,1V is increased, as shown in Fig. 3b. The VTCs show the NMs nearly double (compared to the unipolar case) and at V_{DD} = 5V a rail-to-rail voltage swing is achieved. $I_{stat,1} = I_{min,p}$ is reduced to 200 nA and I_p increases to 3.0 µA. At V_{DD} = 5V, this inverter switches nearly twice as fast and I_{stat} is reduced by ~3.5, resulting in I_p/I_{stat} = 15. Therefore, this inverter is 15 times more 'efficient' than the unipolar resistive inverter (note this is an underestimate as a TFT generally discharges the load capacitance quicker than a resistor). At V_{DD} = 3V, I_p is only 810 nA and I_p/I_{stat} = 4. For V_{DD} = 1V, V_{out} = ~ 0.7V at V_{in} = 1V

and no inversion is possible; the gain is <1 resulting in sub-zero NMs.

In Fig. 3c,g,k the inverter is modelled using the p-type SnO TFT with $(W/L)_p = 20$ ($(W/L)_p/(W/L)_n = 1$). The output currents are no longer matched at $V_{GS} = 5$V but the match improves at lower V_{GS} (Fig. 3c). Fig. 3g shows improved performance at lower voltages resulting in rail-to-rail swing and a NM=44% when $V_{DD} = 3$V. At $V_{DD} = 1$V, the gain is just above unity with a small NM = 4% but $V_{out} > 0.3$V. Interestingly, the NM at $V_{DD} = 5$V also improves, despite a larger mismatch at $V_{GS} = 5$V. Crucially, this shows that matching $I_{min,n}$ and $I_{min,p}$ at the expense of mismatching $I_{max,n}$ and $I_{max,p}$ improves the NMs over a wide range of V_{DD}. Moreover, $I_{stat,1} = I_{min,p}$ is reduced from 200 nA to 40 nA. I_p is reduced to 1.1 µA ($V_{DD} = 5$V) and 350nA ($V_{DD} = 3$V) causing a longer propagation delay. However, the overall efficiency is higher since I_p/I_{stat} is ~26 and ~9 for $V_{DD} = 5$V and $V_{DD} = 3$V respectively. This shows that reducing $(W/L)_p$ from 5 to 1 nearly doubles the efficiency, and improves the NMs. Compared to ~3300 for the ideally matched case, 26 is relatively low, but is still >25-fold improvement over the unipolar resistive inverter. Since the power consumption of recent flexible microprocessors employing resistive load technology is > 99% static [14], a 25-fold reduction in P_{stat} could potentially result in a 25-fold increase in the number of gates. An additional advantage is that $(W/L)_p/(W/L)_n = 1$ reduces the area occupied by the CMOS inverter, as well as parasitic capacitance. Whether these advantages outweigh the complexity of adding the p-type (n-type) material varies for different applications. Note that Si processors operate at higher frequencies since the mobility of crystalline Si is > 100 times higher than for metal-oxides and organics. Combined with the low off-current of Si transistors (resulting in a high I_p/I_{stat}), this means P_{stat} of Si CMOS gates is usually negligible compared to the dynamic power (P_{dyn}) as defined in equation (8). Further note that P_{dyn} scales with f (and therefore I_p) which makes it impossible to optimise I_p/I_{dyn} in equation (9) (for constant V_{DD}, C_L and assuming the input rise time, t_s, is negligible). For this reason the inverter efficiency is defined as I_p/I_{stat}. The type of application also matters, for example in a microprocessor the average number of gates that switch at any time is a relatively low percentage (x in equation (9)) of the total number of gates which reduces P_{dyn}. In less complex systems, a higher proportion of gates might be switching and x will be larger.

$$P_{tot} = P_{dyn} + P_{stat} = x(C_L V_{DD}{}^2 + V_{DD} I_{peak} t_s)f + V_{DD}\frac{I_{stat}}{2} \quad (8)$$

$$\frac{P_{tot}}{V_{DD}} = x(C_L V_{DD} + I_{peak} t_s)f + \frac{I_{stat}}{2} = x I_{dyn} + \frac{I_{stat}}{2} \quad (9)$$

All-oxide CMOS inverter performance

The modelling results were verified experimentally by connecting SnO and a-ISO TFTs to form two all-metal-oxide CMOS inverters with different $(W/L)_p/(W/L)_n$. The first inverter consists of the a-ISO TFT with $(W/L)_n = 20$ and the SnO TFT with $(W/L)_p = 100$. In the second configuration the SnO TFT with $(W/L)_p = 20$ is used. The measured VTCs and CTCs are represented by the dotted lines in Fig4a,b,c,d. The difference between the forward and backward sweeps is caused by the hysteresis of the SnO TFT (Fig. 2b,c).

Fig. 4a,b,c,d show the model fits the measured data well for both configurations across a range of V_{DD}. It should be noted that a correction was applied to account for a reduction in measured $I_{max,p}$ and $I_{min,p}$, caused by hysteresis from sweeping $V_{GS} = V_{in}$. For $(W/L)_p = 20$ and $V_{DD} = 1$V the measured device achieves rail-to-rail swing and outperforms the model due to the reduced $I_{min,p}$. The Supplementary Information provides details on the modelling and hysteresis effects.

Fig. 4f,g,h shows I_p, I_{stat} and I_p/I_{stat} of the two measured devices and perfectly matched inverter for $V_{DD} = [0, 5V]$. By changing $(W/L)_p$ from 100 to 20, I_{stat} is reduced by a factor 5 while I_p is only reduced by 3; I_p/I_{stat} therefore improves by 60%. This confirms that reducing $(W/L)_p$ increases I_p/I_{stat} compared to simply scaling up $(W/L)_p$ inversely with mobility as long as (i) $I_{min,p}$ scales with $(W/L)_p$ and (ii) $I_{min,p}$ is considerably larger than $I_{min,n}$.

Fig. 4h shows I_p/I_{stat} for the perfectly matched CMOS inverter reaches ~3300 for $V_{DD} = 5$V due to the low I_{stat}. For CMOS devices, I_p scales with V_{DD} while I_{stat} remains approximately constant. Therefore, I_p/I_{stat} increases and the inverter becomes more 'efficient' at higher V_{DD}. This key advantage of CMOS over other inverters is quantitively captured by I_p/I_{stat}.

Fig. 4e shows I_p/I_{stat} is ~1 for the (6MΩ) unipolar resistive inverter since I_{stat} =~ I_p as V_{DD} increases. Two other inverter configurations that commonly employ TFTs are shown; an ambipolar inverter [30] and zero-V_{GS} metal-oxide inverter [31]. Both these devices achieve ultralow power consumption (<1 nW) but their use is limited since $I_p/I_{stat} = 1$. The ambipolar inverter operates down to 0.5V where $I_{stat} = 100$ pA but since $I_p = I_{stat}$ the operating frequency is ~10 Hz, limiting the range applications. The device can operate at higher voltages but I_{stat} increases with I_p, as for the unipolar resistive inverter. In this case, the complementary configuration improves the VTCs and NMs but not I_p/I_{stat}. The zero-V_{GS} inverter combines two Schottky-barrier IGZO TFTs. The pull-up TFT operates in saturation with $V_{GS} = 0$V resulting in an ultralow operating current of ~100 pA for $V_{DD} = 2$V. This is similar to operating with a large resistive load (I_p/I_{stat} = ~1) and the switching frequency is once again limited to ~10 Hz. Both the ambipolar and zero-V_{GS} configurations are suitable for ultralow-power, low-frequency applications but not for flexible processors where a high I_p/I_{stat} is required for operation > 1kHz and low P_{stat}.

In Fig. 4i,j the I_p/I_{stat} of two state-of-the-art all-oxide CMOS inverters have been calculated and plotted for comparison [23], [32]. The SnO TFTs reported in these works have an

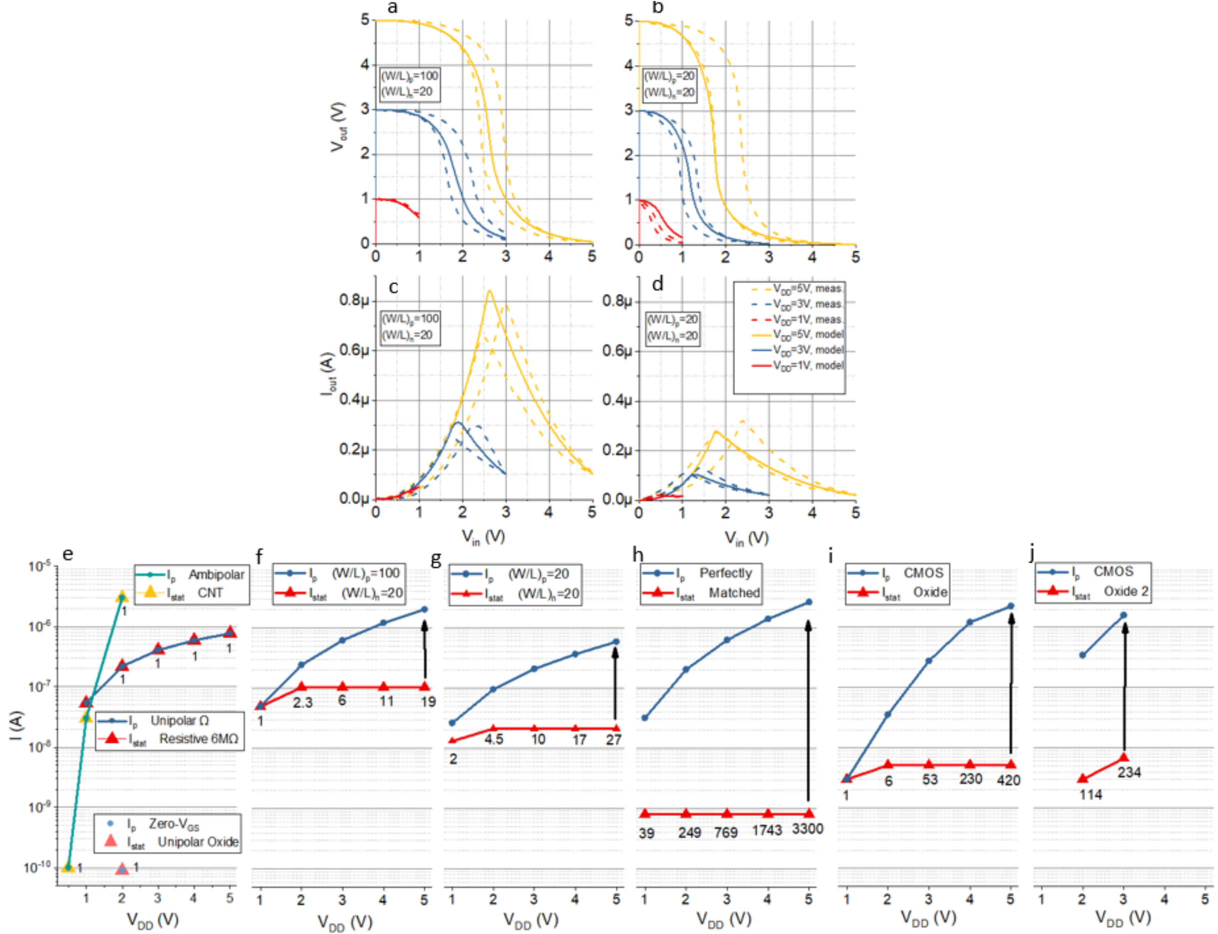

Fig. 4. Measured and modelled (solid line) voltage transfer characteristics for the a-ISO+SnO inverters (a, b) and current transfer characteristics (c, d). Peak, static currents and the ratio between them for V_{DD}=[0,5V] of different inverter configurations (e) unipolar resistive, CNT ambipolar [30], IGZO zero-V_{GS} [31] , (f) CMOS a-ISO+SnO $(W/L)_p/(W/L)_n$=100/20, (g) CMOS a-ISO+SnO $(W/L)_p/(W/L)_n$=20/20, (h) CMOS ISO perfectly matched, (i) CMOS IGZO+SnO [23], (j) CMOS IGZO+SnO [32]

I_{on}/I_{off} of ~10^5 and SS of ~1 V/dec, which are superior to our SnO TFTs (likely due to thin high-quality Al_2O_3 dielectric layers). As expected, I_p/I_{stat} of these inverters is considerably higher but for both devices $(W/L)_p/(W/L)_n$ has been scaled up using the silicon CMOS approach (to 5 and 3 respectively) to simply compensate for the mobility difference. In the next section, we explain how I_p/I_{stat} for these inverters can be improved by scaling $(W/L)_p/(W/L)_n$ optimally.

Optimal geometric aspect ratio

In this work we have shown that reducing $(W/L)_p/(W/L)_n$ can increase I_p/I_{stat} compared to simply scaling up W/L inversely with mobility, while reducing the area. This raises the question whether an optimal $(W/L)_p/(W/L)_n$ exists, which maximises these parameters. Ideally the maximum (V_{GS} = ± V_{DD}) and minimum (V_{GS} = 0V) drain currents of the n-type TFTs, $I_{max,n}$ and $I_{min,n}$, equal the ones of the p-type TFTs, $I_{max,p}$ and $I_{min,p}$. For silicon transistors with full channel depletion $I_{min,p}$ and $I_{min,n}$ are usually similar and independent of (W/L). This means the lower hole mobility is compensated by scaling $(W/L)_p$ up until $((W/L)_pI_{max,p})$ matches $I_{max,n}$ (Fig. 1b,g). As long as $V_{th,p}$ and $V_{th,n}$ are well matched, and the oxide capacitance is uniform, an excellent match of the output characteristics is achieved. As explained previously, this does not work for metal-oxide TFTs since the p-type (SnO) TFT has a high $I_{min,p}$ and low $I_{max,p}$ compared to the n-type (a-ISO) TFT as illustrated in Fig. 1i. Scaling up $(W/L)_p$ brings $(W/L)_pI_{max,p}$ closer to $I_{max,n}$ but increases the gap between $(W/L)_pI_{min,p}$ and $I_{min,n}$. Here we propose the optimal $(W/L)_p$ can be found by setting the ratios $I_{max,n}/(W/L)_pI_{max,p}$ and $(W/L)_pI_{min,p}/I_{min,n}$ equal (assuming $I_{max,p}$ and $I_{min,p}$ correspond to $(W/L)_p$ = 1). As such, a compromise is made between matching minimum and maximum output currents. The optimal $(W/L)_p$ can be found by solving:

$$\frac{I_{max,n}}{\left(\frac{W}{L}\right)_p I_{max,p}} = \frac{\left(\frac{W}{L}\right)_p I_{min,p}}{I_{min,n}} \quad (10)$$

This value is dependent on V_{DD} since the output characteristics vary with V_{DS}. For silicon transistors $I_{min,p}$ no longer scales with $(W/L)_p$ and equals ~ $I_{min,n}$; therefore

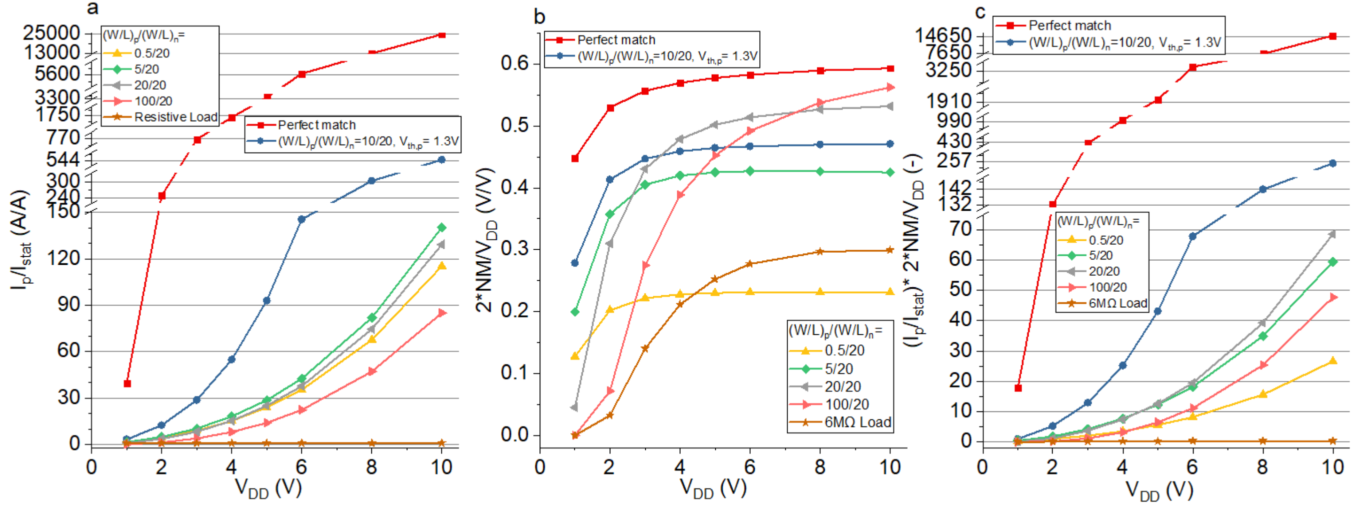

Fig.5. (a) I_p/I_{stat} and (b) normalized noise margin (2*NM/V_{DD}), and (c) I_p/I_{stat} *(2*NM/V_{DD}) for the unipolar resistive load inverter, CMOS ISO-SnO inverter with different (*W/L*) ratios, threshold voltage shifted and perfectly matched cases.

$(W/L)_p I_{min,p}/I_{min,n}$ can be set to ~ 1. This results in an optimal $(W/L)_p$ equal to $I_{max,n}/I_{max,p} = \mu_{sat,n}/\mu_{sat,p}$ as expected:

$$Silicon:\quad optimal\ \left(\frac{W}{L}\right)_p = \frac{I_{max,n}}{I_{max,p}} = \frac{\mu_{sat,n}}{\mu_{sat,p}} \quad (11)$$

For TFTs where $I_{min,p}$ (or $I_{min,n}$) scales with $(W/L)_p$ ($(W/L)_n$), corresponding to the scenarios in Fig. 1c,d,e,h, the following are applicable:

$$Oxide:\quad optimal\ \left(\frac{W}{L}\right)_p = \sqrt{\frac{I_{max,n}}{I_{max,p}} \times \frac{I_{min,n}}{I_{min,p}}} \quad (12)$$

$$Organics:\quad optimal\ \left(\frac{W}{L}\right)_n = \sqrt{\frac{I_{max,p}}{I_{max,n}} \times \frac{I_{min,p}}{I_{min,n}}} \quad (13)$$

By taking the derivative of I_p/I_{stat} w.r.t. $(W/L)_p$ and setting this equal to zero, we show that this expression indeed maximises I_p/I_{stat} (for $(W/L)_p$ >0). The expression for I_p/I_{stat} for a CMOS inverter where both $I_{min,p}$ and $I_{max,p}$ scale with $(W/L)_p$ is given in equation (14). Equation (15) shows that the optimal $(W/L)_p$ from equation (12) sets the top part of the derivative of I_p/I_{stat} w.r.t. $(W/L)_p$ equal to zero. In the Supplementary Information a plot of I_p/I_{stat} versus $(W/L)_p$ is included for the inverter in this work.

$$\frac{I_p}{I_{stat}} = \frac{\dfrac{I_{max,n}\left(\frac{W}{L}\right)_p I_{max,p}}{I_{max,n} + \left(\frac{W}{L}\right)_p I_{max,p}}}{I_{min,n} + \left(\frac{W}{L}\right)_p I_{min,p}} \quad (14)$$

$$\frac{\partial}{\partial\left(\frac{W}{L}\right)_p}\frac{I_p}{I_{stat}} = \frac{I_{max,n}I_{max,p}\left(I_{max,n}I_{min,n} - I_{max,p}I_{min,p}\left(\frac{W}{L}\right)_p^2\right)}{\left(I_{max,p}\left(\frac{W}{L}\right)_p + I_{max,n}\right)^2 + \left(I_{min,n} + I_{min,p}\left(\frac{W}{L}\right)_p\right)^2} \quad (15)$$

It is suggested to calculate the optimal $(W/L)_p$ ($(W/L)_n$) for the maximum required V_{DD}. If $I_{min,n}$ ($I_{min,p}$) is much smaller than other currents in the system, (i.e. for IGZO TFTs $I_{min,n}$ can be ~1fA) it is advised to set $I_{min,n}$ ($I_{min,p}$) equal to the lowest critical current. This method can also be applied to maximise I_p/I_{stat} for Si CMOS inverters. However, the low I_{stat} means that the effect on the overall power consumption will be negligible and it makes more sense to scale $(W/L)_p$ to maximise NMs.

For the a-ISO-SnO inverter with $(W/L)_n = 20$, the optimal $(W/L)_p$ were calculated as 4 and 5 at $V_{DD} = 5$V and $V_{DD} = 10$V respectively. Using the model, I_p/I_{stat} and the NMs were estimated for different $(W/L)_p$. Fig. 5a shows reducing $(W/L)_p$ from 100 to 5, nearly doubles I_p/I_{stat} for $V_{DD} = 5$V and improves by over 60% for $V_{DD} = 10$V. However, reducing $(W/L)_p$ any further from 5 to 0.5 leads to a decrease in I_p/I_{stat} and 5 is therefore the optimal value. Increasing $(W/L)_p$ from 5 to 20 reduces I_p/I_{stat} by only 10%. The perfectly matched and resistive load cases are shown for comparison. It also includes the scenario where $V_{th,p}$ is reduced by 1 V to 1.3 V resulting in a considerable reduction in $I_{min,p}$ and therefore increase in I_p/I_{stat}. This shows changing $(W/L)_p$ makes a noticeable difference but combining it with an optimal $V_{th,p}$ can have significantly greater impact (note the optimal $(W/L)_p$ is 10 in this case). The V_{th} of oxide TFTs is difficult to control as there is no appropriate doping process. It can be improved by reducing the dielectric thickness (and using a high k dielectric), and removing defects between the dielectric and semiconductor interface (i.e. by annealing, interface layers, choice of materials and processing conditions).

NMs are equally important and modelled as a function of $(W/L)_p$ (Fig. 5b) which confirms that reducing $(W/L)_p$ from 100 to 20 increase the NMs for $V_{DD} < 8$V. For $(W/L)_p = 5$ the NMs improve for $V_{DD} < 3$V but a further reduction to $(W/L)_p = 0.5$ lowers them for all V_{DD}. NMs for the perfectly matched and resistive load are included for reference.

To take into account both I_p/I_{stat} and the NMs, a new dimensionless parameter is introduced, (I_p/I_{stat})*NM/(V_{DD}/2), and plotted in Fig. 5c. This shows that for $V_{DD} < 5$V the

TABLE 1. Suggested optimal geometric aspect ratios **Hysteresis

Channel p	Channel n	V_{DD}	Total area $(W/L)_p+(W/L)_n$	$(W/L)_p$ $(W/L)_n$	$I_{min,p}$ (A) $I_{min,n}$ (A)	$I_{max,n}$ (A) $I_{max,p}$ (A)	I_p/I_{stat}	Ref	Total area $(W/L)_p+(W/L)_n$	$(W/L)_p$ $(W/L)_n$	$I_{min,p}$ (A) $I_{min,n}$ (A)	$I_{max,n}$ (A) $I_{max,p}$ (A)	I_p/I_{stat}
Actual values									Suggested optimal values (*perfectly matched*)				
SnO	a-ISO	10V	120	100 20	200n=500 0.4n	40µ=1.3 31µ	85 (110**)	This work	25 (*40*)	5 (*20*) 20	10n=25 0.4n	40µ=25 1.6µ	148 (*25000*)
		5V	40	20 20	40n=100 0.4n	5.4µ=4 1.3µ	26 (28**)		24 (*40*)	4 (*20*) 20	8n=20 0.4n	5.4µ=21 0.26µ	30 (*3300*)
SnO	ZnO	8V	6	5 1	750n=2500 0.3n	2.6µ=1 2.7µ	1.7	[28]	1.1 (*2*)	0.1 (*1*) 1	15n=50 0.3n	2.6µ=50 0.05µ	3.5 (*2200*)
SnO	IGZO	5V	7	6 1	5n=50 0.1n	3µ =0.4 8µ	420	[23]	1.5 (*2*)	0.5 (*1*) 1	0.4n=4 0.1n	3µ=4 0.7µ	1100 (*7500*)
SnO	IGZO	2V	4	3 1	3n=30 0.1n	0.8µ=1.3 0.6µ	114	[32]	1.66 (*2*)	0.66 (*1*) 1	0.66n=6.6 0.1n	0.8µ=6.6 0.12µ	137 (*2000*)
Pentacene organic	$F_{16}CuPc$ organic	1.5V	36.6	3.3 33.3	1p=0.01 0.1n	0.6µ=2 0.3µ	1980	[11]	5.7 (*6.6*)	3.3 2.4 (*3.3*)	1p=0.14 7p	42n=0.14 0.3µ	4600 (*75000*)

performance of $(W/L)_p = 5$ and $(W/L)_p = 20$ is very close (and nearly double that of $(W/L)_p = 0.5$ and $(W/L)_p = 100$). For $V_{DD} > 5V$ $(W/L)_p = 20$ outperforms $(W/L)_p = 5$ as the NM increases more than I_p/I_{stat}. This shows that $(W/L)_p = 5$ provides a bottom line which maximises I_p/I_{stat} but that it might be worth increasing $(W/L)_p$ to above this value to increase NMs further. Alternatively a larger $(W/L)_p$ might be required to achieve higher switching frequency. In this case we suggest to increase $(W/L)_n$ first (and therefore $I_{max,n}$) and recalculate the corresponding optimal $(W/L)_p$.

Table 1 shows the actual and suggested optimal $(W/L)_p/(W/L)_n$, corresponding output currents, and I_p/I_{stat}. For the inverter in Fig. 4i I_p/I_{stat} can almost be tripled by choosing the optimal $(W/L)_p/(W/L)_n$, while reducing the total area. This represents a straightforward method to geometrically optimise the inverter performance, provided the maximum and minimum output currents of the n- and p-type TFTs are measured (or modelled). Calculating NMs is more difficult but can be obtained by adjusting the modelling parameters in equations (1) and (2). I_p/I_{stat} for the inverter in Fig. 4j is close to the optimal value and therefore the gains are limited. Optimisation based on NMs and switching speed is likely to be more important in this case. For the SnO-ZnO CMOS inverter [28] I_p/I_{stat} is only 1.8. This inverter has excellent NMs (>60%), but I_p/I_{stat} shows that the inverter efficiency is only marginally better than the unipolar resistive inverter. The last row contains an estimate for the optimal $(W/L)_p/(W/L)_n$ for an organic complementary inverter for which the p-type TFT outperforms the n-type. However, note that for this inverter I_p/I_{stat} is already > 1000, meaning it is unlikely that P_{stat} is the dominant factor.

Conclusions (and outlook for all-oxide CMOS inverters)

We have proposed an optimal $(W/L)_p/(W/L)_n$ that maximises I_p/I_{stat} and can be applied universally to silicon, metal-oxide and organic complementary inverters. Notably, our results show that reducing *W/L* of metal-oxide p-type TFTs increases I_p/I_{stat} while reducing the area compared to simply scaling up *W/L* inversely with mobility. A high inverter efficiency is critical to reduce P_{stat} and increase the gate density of (flexible) processors; we have shown that I_p/I_{stat} of state-of-the-art all-oxide CMOS inverters can be maximised by adopting the optimal $(W/L)_p/(W/L)_n$. In this way n- and p-type TFTs with significant differences in performance can be matched optimally without changing the intrinsic properties such as V_{th}, SS, I_{on}/I_{off} and mobility.

Despite the clear need for all-oxide CMOS inverters required for low-cost flexible electronics, only a handful have been reported. For ambipolar, unipolar resistive and zero-V_{GS} configurations $I_p/I_{stat} = 1$; they simply cannot provide the necessary reduction in I_{stat} without sacrificing switching speed. The high I_{off} of SnO TFTs remains a bottleneck, but has reached a sufficiently low level to reduce I_{stat} by at least 100-fold over unipolar logic for V_{DD} ~ 3-5V. While this might seem small compared to a ratio of ~3300 for a perfectly matched CMOS inverter, it makes a significant difference for natively flexible microprocessors. The recently reported microprocessor containing 18,334 NAND2 gates with unipolar n-type resistive load logic operates at a maximum clock-frequency of 29kHz [14]. The power consumption is ~21mW, of which >99% is static. Based on these figures and $V_{DD} = 3V$, we estimate $I_p = I_{stat,1}$ for each gate to be ~750 nA which is close to I_p values reported in this work and recent literature. This shows that replacing the resistive load with a state-of-the-art SnO TFT, combined with the correct *W/L* ratio, could reduce I_{stat} by a factor > 200 at $V_{DD} = 3V$ (constant I_p). Since P_{stat} is the dominant factor, this reduces total power by nearly 200-fold, allowing an increase in the number of gates on the chip to over a million, approaching VLSI standards. This shows that while the performance of current SnO TFTs is still significantly behind their n-type counterpart, they are already able to reduce P_{stat} to such a level that it is no longer the dominant component. A further reduction of I_{off} is welcome but will not affect the overall power consumption significantly as the dynamic power will start to dominate. To realise a flexible microprocessor employing all-oxide CMOS technology it is critical to improve the stability (hysteresis) and repeatability of SnO TFTs.

Methods

Device Fabrication. The CMOS inverters are formed by interconnecting a bottom-gate staggered n-type a-ISO TFT to a bottom-gate staggered p-type SnO TFT. The schematic structure of each TFT is shown in Fig. 2d,i. The substrate of the n-type TFT is glass on which a 100 nm Cr bottom electrode layer is deposited using a Metallifier Sputter Coating System (Precision Atomics). The gate electrode was patterned using Cr etchant. On top of this a 180 nm Al_2O_3 dielectric layer (47 nF/cm^2) was deposited at 150°C by atomic layer deposition (MVSystems). After this the 10nm ISO (10 wt% Si) channel layer was deposited by rf-sputtering (MVSystems) at an oxygen-to-argon flow ratio of 16.7%, rf power of 150 W, and deposition pressure of 4 mTorr. The top layer is a 100 nm Mo deposited by the Metallifier Sputter Coating System to form source/drain (S/D) electrodes. Patterning of this layer was done by reactive ion etching (Philips RIE) at a power of 100W and pressure of 150mTorr. All layers were patterned with AZ5214E photoresist. The a-ISO devices were annealed for two hours in ambient air at 200 °C to improve the performance. The *W/L* ratio of the devices was 20 with a constant channel length of 20 μm.

For the p-type TFTs, 10nm SnO layers were formed on thermally-grown SiO_2 on a p^+-Si substrate by ALD (Beneq TFS-200) at 170 °C using a tin(II) amide precursor. The p^+-Si and SiO_2 (~ 200 nm) were used as a common gate electrode and a gate insulator (12 nF/cm^2), respectively. A 100 nm Au layer was deposited as S/D electrodes using a thermal evaporator (Edwards E306A). Finally, a 70nm passivation layer of Al_2O_3 was deposited. The devices were annealed for two hours at 200 °C in ambient air. The active layers and S/D electrodes were patterned by a lift-off process using AZ5214E photoresist. The *W/L* ratio varied from 20 to 100 with a constant channel width of 1000 μm.

The maximum fabrication temperature of the above processes is 200 °C resulting in low fabrication costs and the ability to deposit on flexible substrates such as DuPont Kapton HN sheet. A further reduction in annealing temperature to 170 °C should be possible by increasing the annealing time. Note a p^+-Si substrate with SiO_2 was used for the p-type device for ease of manufacturing but in the future this could easily be replaced by a glass or flexible substrate with oxide dielectric.

Device Characterisation. The electrical performance of the TFTs and the inverters were analysed using a Keithley 4200 semiconductor characterization system. A six probe configuration was used to interconnect the gate electrodes of different n- and p-type TFTs and feed in a common input voltage. Similarly the drain electrodes were interconnected to measure the output voltage. This setup allows to connect p-type TFTs with different *W/L* ratios to the same n-type TFT and isolate the effects of changing $(W/L)_p/(W/L)_n$.

Data Availability. The datasets generated during and/or analysed during the current study are available in the Cambridge University Data Repository (http://www.repository.cam.ac.uk/).

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