Separately contacted monocrystalline silicon double-layer structure with an amorphous silicon dioxide barrier made by wafer bonding

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Abstract.

A double-layer of monocrystalline silicon separated by a 23.5 nm silicon-dioxide barrier is fabricated by bonding two silicon-on-insulator wafers with oxidized surface layers. The two layers are separately contacted allowing transport measurements through individual layers and a bias voltage to be applied between the layers. Four-terminal magnetotransport measurements at cryogenic temperatures on electrons generated close to the central oxide barrier show reasonable mobility.

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1. Introduction

Research into coupled 2-dimensional systems [1] and coupled quantum dots [2] are generally based on two dimensional electron gasses (2DEGs) afforded by epitaxially grown III-V heterostructures. Although such structures provide high mobility electrons, extending the complexity of the structures both vertically and laterally is limited by bounds imposed by the choice of compatible materials and difficulties involved with post-lithographic growth. On the other hand, recent advances in wafer bonding and layer transfer techniques offer many opportunities for creating new heterostructures. Examples include silicon-on-insulator (SOI) where a monocrystalline layer of silicon can be achieved on an amorphous layer of silicon dioxide [3, 4]. Furthermore, the layer transfer process can be repeated to make multilayers of silicon and silicon dioxide allowing more complex structures to be engineered [5]. The technique has been successfully applied to incorporating lithographed components such as gates beneath the active crystalline silicon layer [6] and to creating vertical double-SiO_2-barrier tunnelling devices [7, 8]. Since silicon dioxide is highly compatible with standard processing techniques and has good dielectric properties, multilayers of silicon and silicon dioxide may provide an ideal platform for creating strongly coupled but independently controllable multilayer systems.

Here, we examine low-temperature in-plane transport in a double-layer crystalline silicon system with amorphous SiO_2 barriers on either side and in between the two silicon layers, to assess the suitability of such structures for quantum devices and physics experiments. Our structure is formed by bonding two SOI wafers with oxidized surfaces which fuse to form the central barrier. Measurements of Shubnikov de Haas (SdH) oscillations and their dependence on gate voltages and interlayer-bias confirm that 2DEGs are generated at the expected positions in the structure and have reasonable mobility.

2. Sample Preparation

In order to obtain one wafer with a double-layer of monocrystalline silicon, two SOI wafers were prepared [Fig. 1(a)(i)]. Commercially procured (100) SIMOX (Separation by IMplantation of OXygen) wafers from the same batch were used with no additional processing aimed at improving the quality of the wafers [9]. Repeated thermal oxidation and surface oxide removal with HF etching were used to achieve the desired SOI thickness ($\sim$49 nm). The two wafers were then thermally oxidized again to create surface oxide layers ($\sim$16 nm). The wafers were pre-bonded under vacuum [Fig. 1(a)(ii)], using the orientation flats for alignment, and then annealed at 1000 °C in N_2 (g) for 3 hours to fuse the two surface oxide layers [Fig. 1(a)(iii)]. To access the double-layer for characterization and device processing, one side of the bonded pair was thinned, ending in a KOH etch to remove the silicon substrate where the upper buried oxide (BOX) acts as an etch-stop [Fig.1 (a)(iv)].

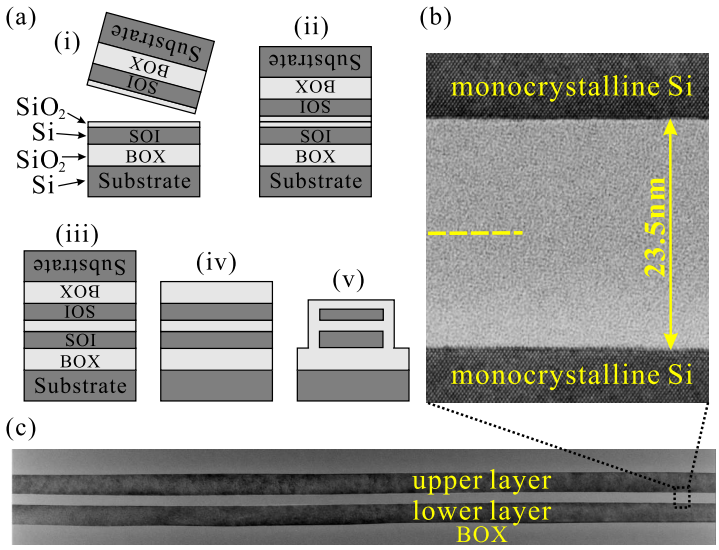

Figure 1. (Colour Online)(a) Preparation. (i) Two SOI wafers are prepared with oxidized surface layers. (ii) Wafers are pre-bonded in vacuum. (iii) The bonded pair is annealed at 1000 °C to make the bond permanent. (iv) The sacrificial silicon substrate is removed. (v) The double-layer can be processed as normal following the chemical removal of the BOX on the surface. (b) Close up TEM image around the bonded interface (marked by the dashed horizontal line), taken following step (iv). (c) TEM image taken over a wide area.

Cross-sectional transmission electron microscopy (TEM) images were then taken [Figs. 1(b) and 1(c)] to assess the resulting structure. No feature could be found at the bonded interface indicating the formation of a well-fused SiO_2 barrier layer separating the two monocrystalline layers of silicon. The thickness was found to be uniform at 23.5nm. Grazing incidence X-ray diffraction measurements [10] were also performed. Two distinct sets of diffraction peaks were observed. Their sharpness and their incident angle dependence confirmed the monocrystallinity of the two layers and their relative depth. The in-plane angular misalignment between the two wafers was found to be 0.145°.

For device fabrication, the exposed BOX was selectively removed by HF etching. Reactive ion etching was used to cut the double-layer structure into Hall bars [Fig. 2(a)] and this was followed by thermal oxidation to create a gate oxide layer on the surface and also to oxidize the mesa edges [Fig. 1(a)(v)]. Regions at the end of each Hall-bar-arm were then implanted with phosphorus ions at two different energies chosen so that the resulting dopant distribution has peaks in the upper and lower-layers and a minimum in the SiO_2 barrier. After rapid thermal annealing to activate the dopants, sections of the implanted regions were stripped of their surface SiO_2 and upper silicon layer. Holes were then etched in the oxide and the doped regions were contacted with evaporated aluminium metal [Fig. 2(b-d)]. The expected layer thicknesses for the final device are: lower silicon layer (t_{LL}) = 42 nm, SiO_2 barrier (t_{B}) = 23.5 nm, upper silicon layer (t_{UL}) = 24 nm and front-gate oxide (t_{FOX}) = 34 nm.

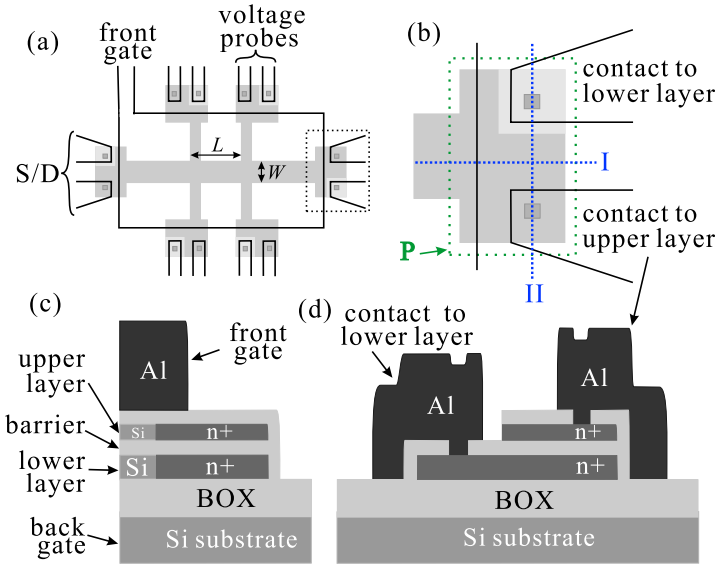

Figure 2. (Colour online). (a) Sample geometry of a Hall-bar sample ($L = 50$ μm, $W = 20$ μm) used for 4-terminal measurements. (b) Close up diagram of a source/drain contact. Region marked P is implanted with phosphorus. (c) Cross-section through line marked I in (b). Regions marked n+ in darker grey are implanted with P. (d) Cross-section through line marked (II) in (b). Layers are selectively removed to independently contact the upper and lower-layers as schematically shown.

3. Transport

After testing the operation of the front and back gates at room temperature, transport measurements were performed with the sample at the base temperature of a 1.4K crysostat. Two terminal measurements were made, operating the device as a metal-oxide-semiconductor (MOS) transistor with two channels (upper and lower). A schematic diagram of the experimental setup is shown in Fig. 3(c). Figures 3(a) and 3(b) show the drain current through the upper and lower-layers ($I_{\rm UL}$ and $I_{\rm LL}$ respectively) with a bias voltage of 10 mV on both contacts as a function of front-gate voltage ($V_{\rm FG}$) taken at different values of back-gate voltage ($V_{\rm BG}$) which is the voltage applied to the substrate. Grey-scale plots of the same data are shown in Figs. 3 (d) and 3(e). Regions in the $(V_{\rm FG}, V_{\rm BG})$-plane can be divided up as schematically shown in Fig. 3(f) depending on which channel is conducting. Diagrams (i), (ii) and (iii) show schematic band diagrams corresponding to the positions marked.

At (i) where $V_{\rm BG}$ is negative and $V_{\rm FG}$ is positive, a 2DEG is generated at the Si/SiO_2 interface closest to the front gate. The upper-layer therefore conducts and the lower-layer does not. Similarly at (ii), a 2DEG is generated in the lower-layer at the interface closest to the back gate and consequently, the lower-layer conducts but the upper-layer does not. Here at (ii), since there are no subbands energetically available for occupation between the conducting channel and the front-gate, $I_{\rm LL}$ increases strongly as $V_{\rm FG}$ is increased, until the front channel starts to occupy, eventually leading to a situation depicted for (iii) where both upper and lower channels conduct. When both channels

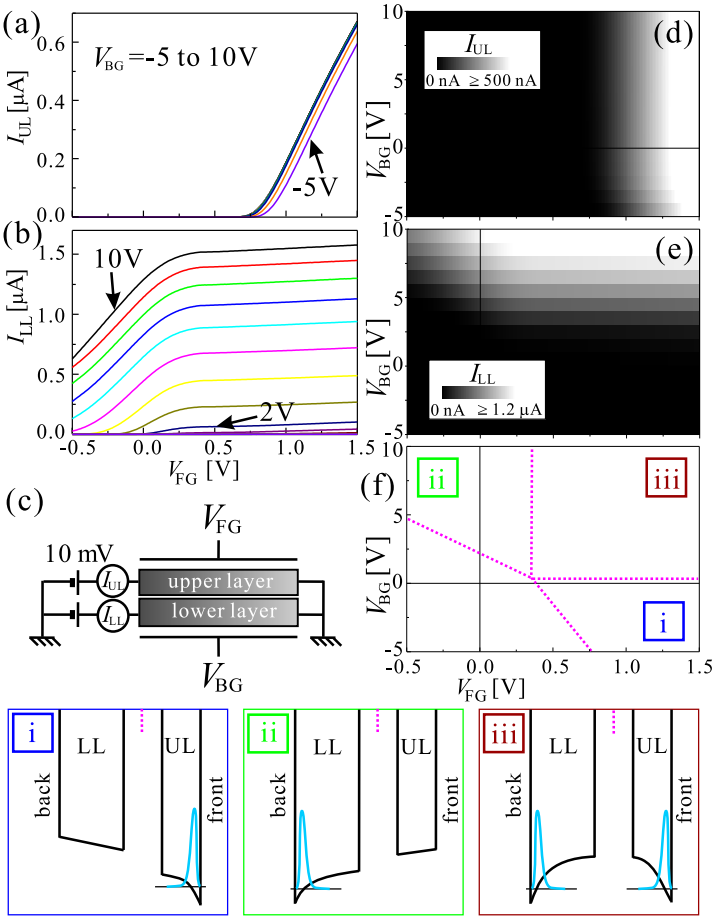

Figure 3. (Colour online) (a) and (b) show I_{UL} and I_{LL} respectively at different values of V_{BG} between 10 and -5 V at 1 V intervals. (c) Schematic of the experimental setup. (d) and (e) show grey-scale plots of data in (a) and (b). (f) A schematic diagram demarcating different regions of the (V_{FG}, V_{BG})-plane. Diagrams (i), (ii) and (iii) are schematic band diagrams corresponding to regions marked in (f). Vertical dotted lines mark the bonded interface.

are conducting, I_{UL} is relatively unaffected by V_{BG} due to the screening provided by the 2DEG at the rear interface. Similarly, the 2DEG in the upper-layer screen the effect of V_{FG} on I_{LL}. These results confirm that electrons are generated in the expected layers. However, in these measurements, the wavefunctions of the electronic subbands involved in transport are distant from the bonded interface, and if there are adverse effects due to the bonding process, we would expect them to be most pronounced when the electrons are close to the bonded interface. In order to generate electrons close to the bonded interface, it is necessary to apply interlayer bias.

4. Interlayer Bias

When a positive front-gate voltage V_{FG} is applied to generate a 2DEG in the upper-layer, the 2DEG in the upper-layer can be used as a gate metal to the lower-layer where

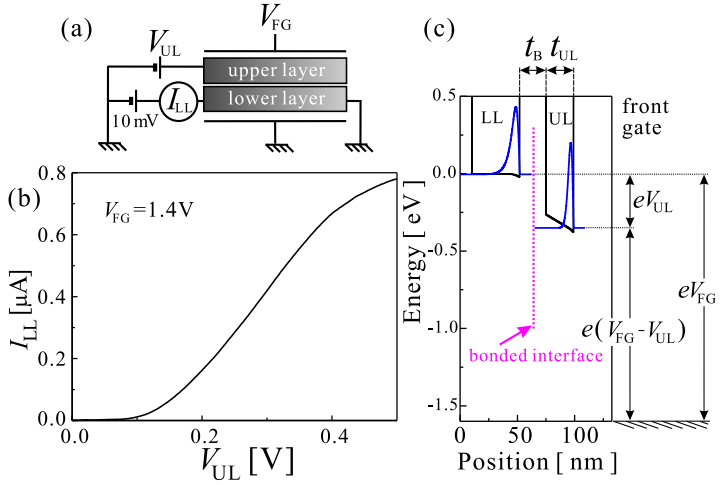

Figure 4. (Colour online). (a) A schematic of the setup used for (b). (b) Current through the lower-layer I_{LL} as a function of the voltage applied on the upper-layer V_{UL} (V_{FG} = 1.4V, V_{BG} = 0V). (c) Band diagram illustrating the effect of interlayer-voltage. Potentials and wavefunctions in the two layers are calculated separately using experimental densities at V_{UL} = 0.35 V, V_{FG} = 1.6 V.

the barrier acts as the gate oxide [Fig. 4(a)]. Figure 4(b) shows the current through the lower-layer I_{LL} as a function of the voltage applied to an upper-layer contact (V_{UL}) (with all other upper-layer contacts floating), clearly indicating gating action. Since a bias is applied between the two layers, a potential gradient is created in the barrier, pulling electrons close to the barrier containing the bonded interface [Fig. 4(c)].

In order to gain information about the electrons in this channel, 4-terminal magnetotransport measurements were performed. Clear SdH oscillations were observed [Fig. 5(a)] with their frequency being tuned by V_{UL} as expected. The electron density obtained from the SdH oscillations as a function of V_{UL} allows us to extract the capacitance between the 2DEG in the upper-layer and the the 2DEG in the lower-layer. We find this interlayer capacitance to have a value of C_{IL}=1100 μFm^{-2} which is consistent with an estimate using

$$C_{IL} \approx \left(\frac{t_{UL}}{\epsilon_0 \epsilon_{Si}} + \frac{t_B}{\epsilon_0 \epsilon_{SiO_2}} \right)^{-1} \quad (1)$$

giving a value of 1100 μFm^{-2} with expected layer thicknesses, where $\epsilon_{Si} = 11.9\epsilon_0$ and $\epsilon_{SiO_2} = 3.9\epsilon_0$ are the permittivities of silicon and silicon dioxide respectively, confirming the position of this 2DEG in the structure [Fig. 4(c)]. Figure 5 (b) shows the mobility calculated from the zero field resitivity and sheet density. At V_{UL} = 0.45 V, the electron sheet density in the lower-layer was 3.6 $\times 10^{15}$ m^{-2} with a reasonable mobility [11] of $\mu = 0.72\,\mathrm{m^2V^{-1}s^{-1}}$.

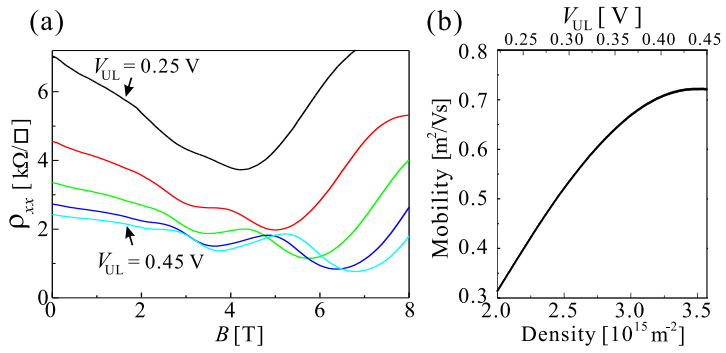

Figure 5. (Colour online). (a) Longitudinal resistivity ρ_{xx} of the lower-layer (V_{FG} = 1.6V, V_{BG} = 0V) taken at different values of V_{UL} between 0.25 and 0.45 V at intervals of 0.05 V. (b) Mobility extracted from data in (a).

5. Summary

In summary, we have demonstrated low-temperature in-plane transport in a separately contacted double-layer monocrystalline silicon device with amorphous SiO_2 barriers fabricated by bonding SOI wafers. The applicability of standard device processing procedures and the quality of the resulting two-dimensional carriers show that these structures can be readily used as a basis for investigating multilayer structures with 3-dimensioanal complexity including separately controlled and contacted but electrostatically coupled systems.

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